Multi-band LC VCO 8-11.3GHz
PMCC_VCOMB12G

IP MACRO **Datasheet Rev 1.2**

Process: 65nm CMOS

DESCRIPTION

PMCC_VCOMB12G is a low noise multi-band differential LC voltage controlled oscillator (VCO). The IP block consists of four one-at-a-time selectable VCOs with center frequencies at 8.5GHz, 10.0GHz, 10.7GHz and 11.1GHz. These frequencies can be tuned using a differential fine and coarse tuning ports. The typical phase noise is below -113dBc at 1MHz offset. The output is CML differential.

The biasing currents are programmable within +/-30% for operational margin estimation in production. Layout is designed using IBM CMOS10LPE 5_01_00_01_LD metal stack. Control functions and layout configuration can be customized upon special agreement.

FEATURES

- Phase noise below -113dBc
- Single 1.2V Power Supply
- VCO center frequencies 8.5GHz, 10.0GHz, 10.7GHz, 11.1GHz
- Each VCO frequency tuning ±8%
- Stand-by mode
- Adjustable (+/-30%) reference current

APPLICATIONS

- Phase-locked loops
- CMU for fiber optic applications
- Reference clock generators

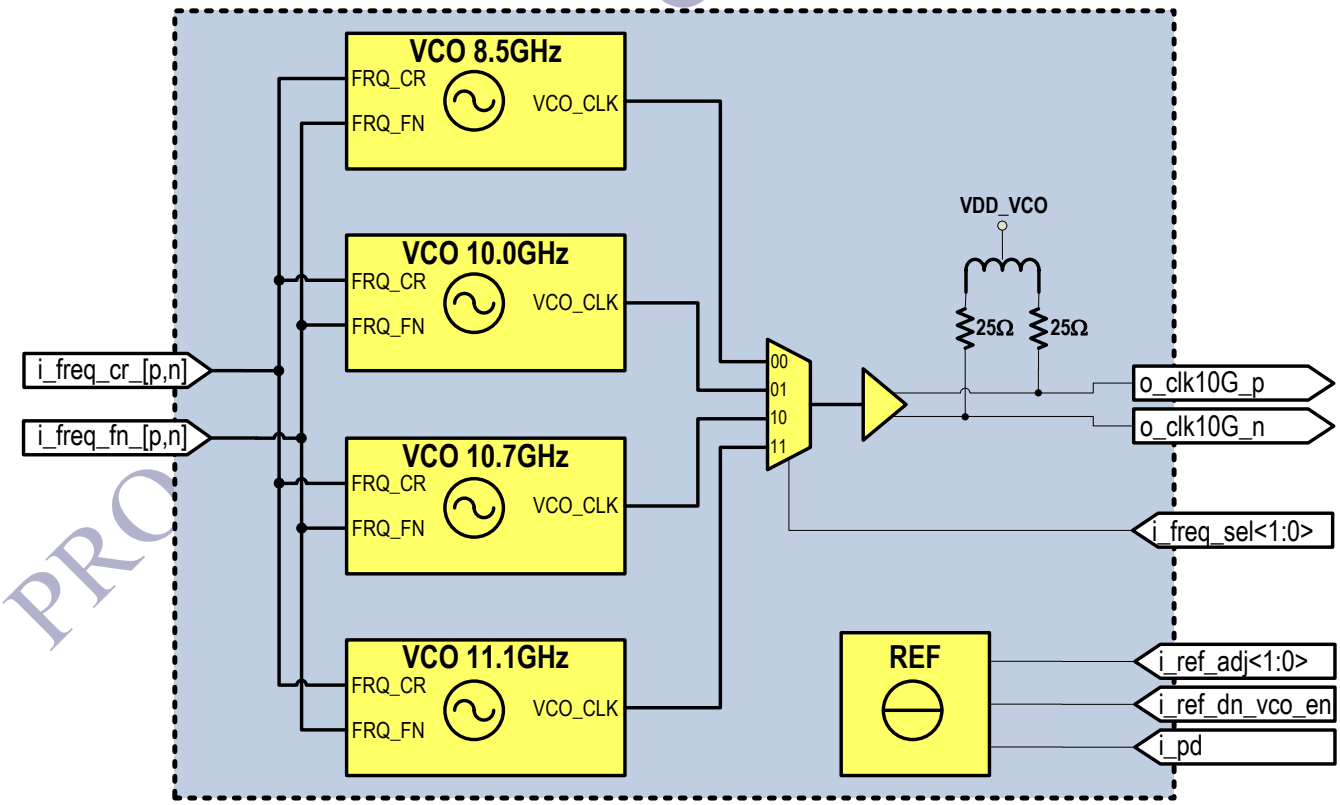


Figure 1. PMCC_VCOMB12G Block Diagram

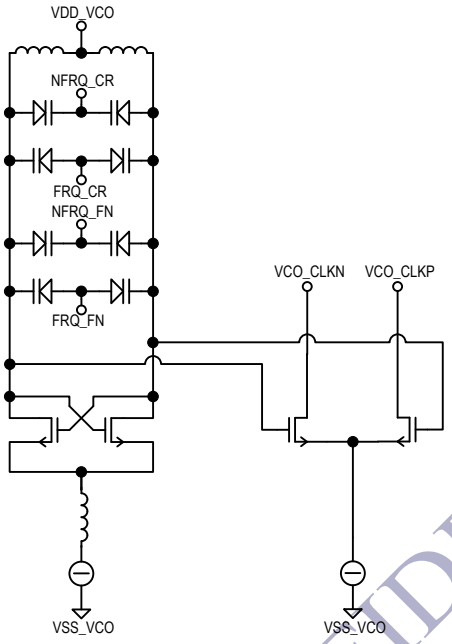


Figure 2. VCO equivalent schematic

Table 1. Pin Descriptions

Name	Pin #	Description	Type
o_clk10G_p		VCO output. Negative polarity	AO
o_clk10G_n		VCO output. Positive polarity	AO
i_freq_cr_p		Coarse VCO tuning port. Positive polarity	AI
i_freq_cr_n		Coarse VCO tuning port. Negative polarity	AI
i_freq_fn_p		Fine VCO tuning port. Positive polarity	AI
i_freq_fn_p		Fine VCO tuning port. Negative polarity	AI
i_freq_sel<1:0>		Input for selecting the VCO frequency	DI
i_ref_dn_vco_en		VCO biasing current adjustment polarity	DI
i_ref_adj<1:0>		VCO biasing current adjustment	DI
i_pd		VCO power down	DI
VDD	C1, C4	1.2V analog power supply	PW
VDD_VCO	A2, A3, A4, B3	1.2V analog power supply for VCO	PW
VSS	C2, C5	Ground for analog circuits	GD
VSS_VCO	A5, B2, B4	VCO ground	GD

Note: AI – Analog input, DI – digital input, AO – analog output, PW – power, GD – ground

Table 2. Electrical absolute maximum ratings

Description	Min	Max	Units
Power supply VDD	-0.5	1.5	V
Power supply VDD_VCO	-0.5	1.5	V
Junction temperature	-55	125	ºC
End Of Life (EOL)	10		years

DC Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes
Power Supply					
Power Supply (VDD)	1.14	1.20	1.26	V	
Power Supply (VDD_VCO)	1.14	1.20	1.26	V	
Power Supply Current		11.5		mA	
Inputs					
Logic control high level	0.9	1.2	1.32	V	
Logic control low level		0.0	0.32	V	
Frequency Coarse Tuning Voltage (DIFF)	-1.2		1.2	V	Differential tuning port.
Frequency Fine Tuning Voltage (DIFF)	-1.2		1.2	V	Differential tuning port.
Outputs					
Termination Resistance at the Output		25		Ω	Single ended, measured at DC.

NOTE: Main operation mode.

Table 4. AC Electrical Specifications

Output	Parameter	Symbol	Min.	Typ.	Max.	Units
Clock outputs **o_CLKO10GP** **o_CLKO10GN**	**Central frequency of 8.5GHz VCO**		8.31	8.56	8.88	GHz
	Central frequency of 10.0GHz VCO		9.81	10.13	10.50	GHz
	Central frequency of 10.7GHz VCO		10.45	10.78	11.17	GHz
	Central frequency of 11.1GHz VCO		11.07	11.41	11.82	GHz
	Tuning range of 8.5GHz VCO		-11.0		13	%
	Tuning range of 10.0GHz VCO		-10.0		11.2	%
	Tuning range of 10.7GHz VCO		-9.7		11.0	%
	Tuning range of 11.1GHz VCO		-9.3		10.5	%
	Impedance at 10GHz			50		Ω
	Output swing, single ended			700		mV, p-p
	Output common mode			1155		mV
-	**KVCO (Coarse)**	Kvco	679		805	MHz/V
-	**KVCO (Fine)**	Kvco	153		174	MHz/V
Tuning port (Coarse) **i_freq_cr_p** **i_freq_cr_n**	**Input capacitance**	Cincr	3.4	3.6	3.8	pF
Tuning port (Fine) **i_freq_fn_p** **i_freq_fn_n**	**Input capacitance**	Cinfn	0.75	0.85	1	pF

Table 5. PMCC_VCOMB12G Frequency Selection Truth Table

i_freq_sel<0>	i_freq_sel<1>	Selected frequency, GHz
0	0	8.5
1	0	10.0
0	1	10.7
1	1	11.1

Table 6. Reference Current Adjustment Truth Table

i_ref_adj<0>	i_ref_adj<1>	i_ref_dn_vco	i_pd	Current Adjustment, %
1	1	0	0	-30
0	1	0	0	-20
1	0	0	0	-10
0	0	0	0	0
0	0	1	0	0
1	0	1	0	+10
0	1	1	0	+20
1	1	1	0	+30

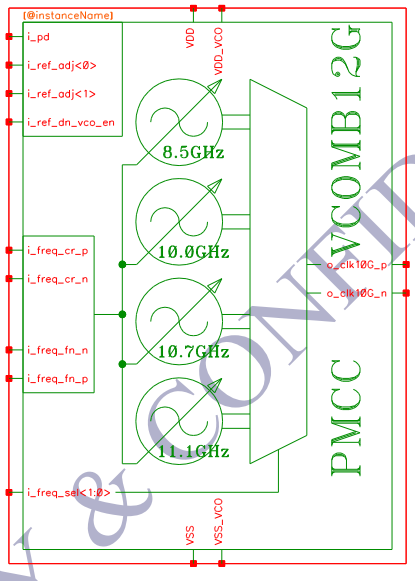


Figure 3. Macro schematic symbol

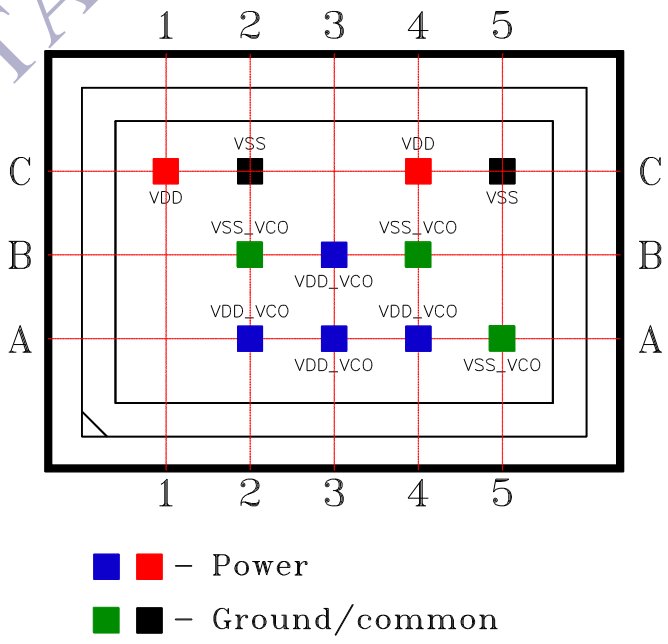


Figure 4. Bump-out diagram

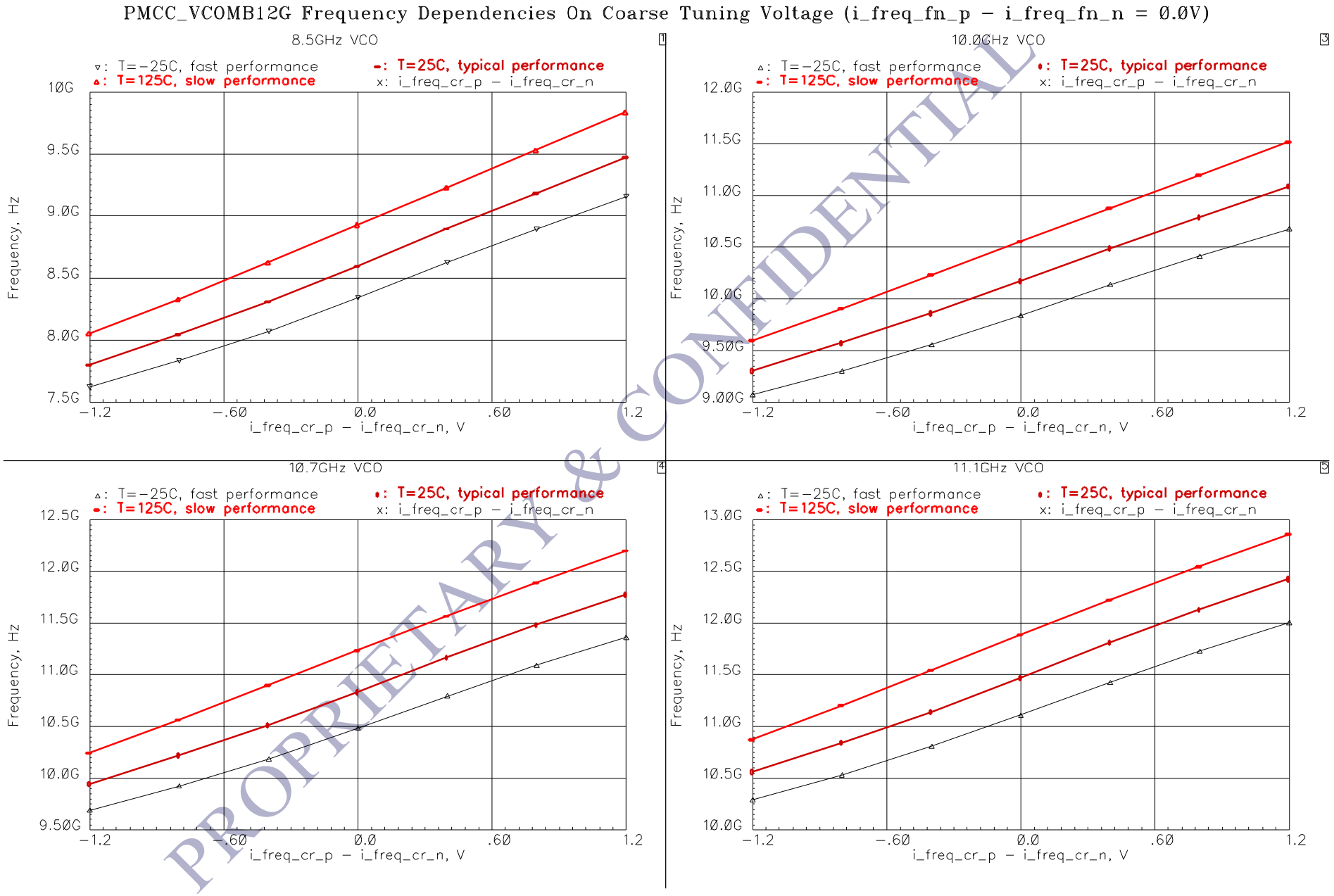


Figure 5. PMCC_VCOMB12G Frequency Dependencies on Coarse Tuning Voltage (i_freq_fn_p – i_freq_fn_n = 0V)

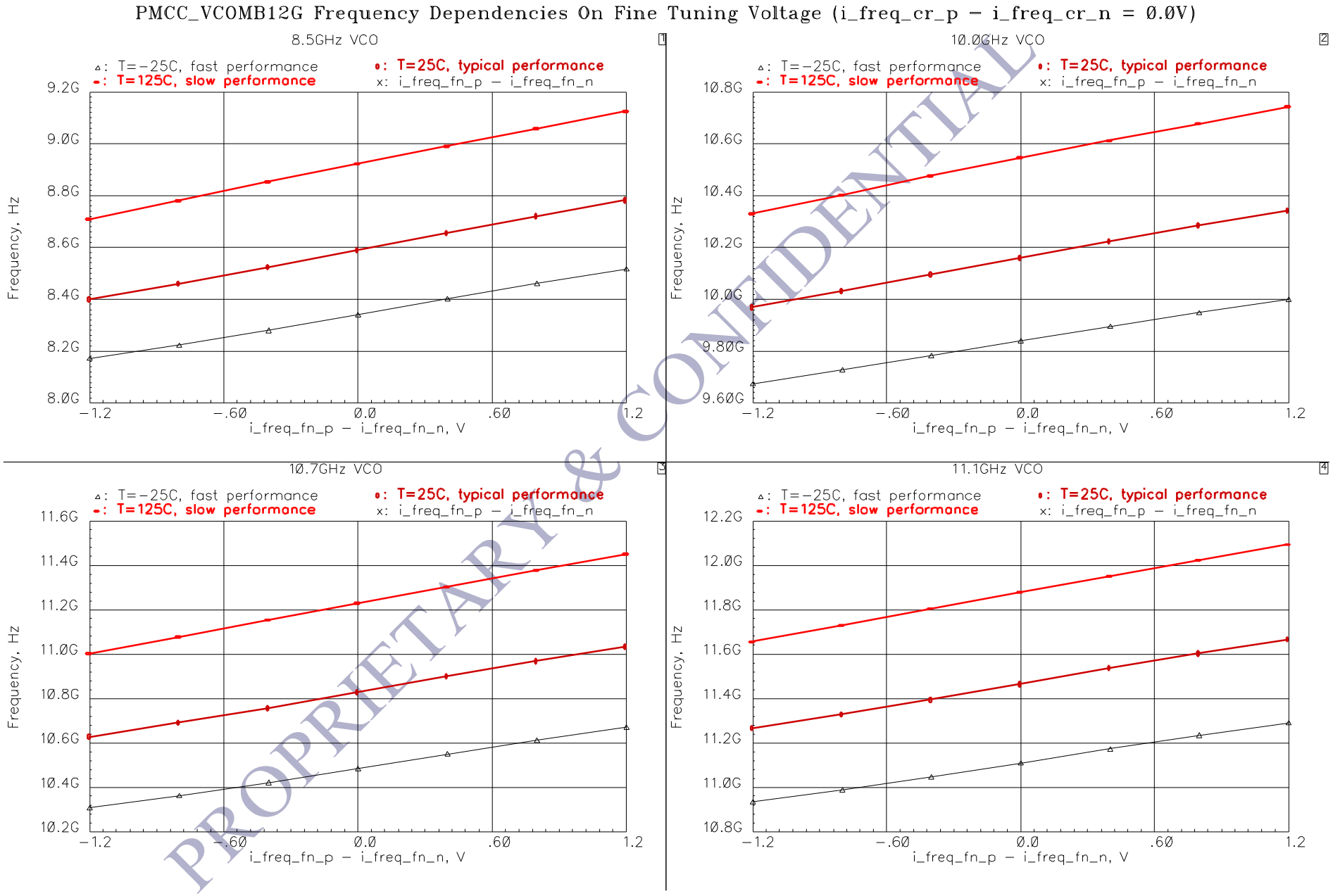


Figure 5. PMCC_VCOMB12G Frequency Dependencies On Fine Tuning Voltage (i_freq_cr_p – i_freq_cr_n = 0.0V)

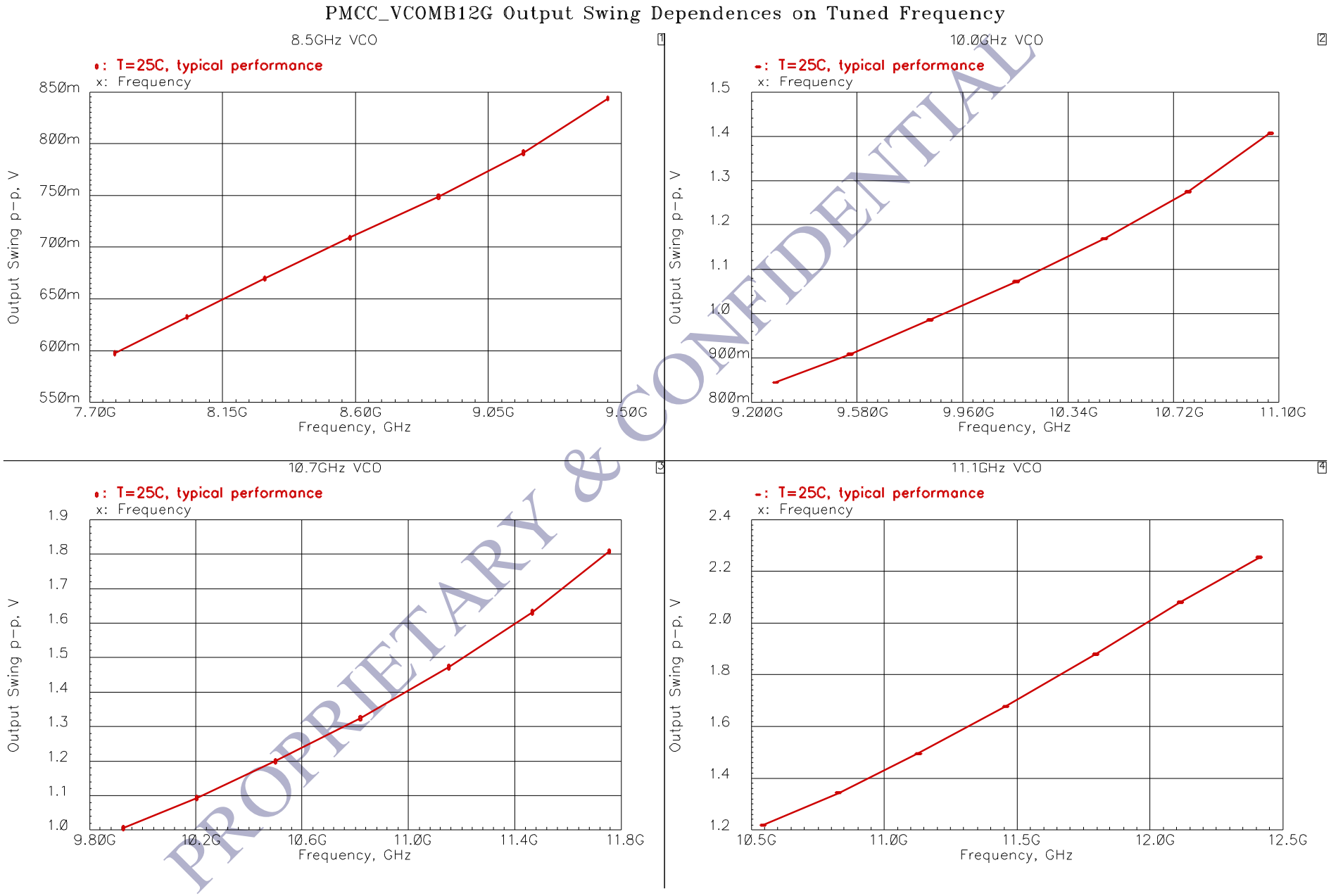
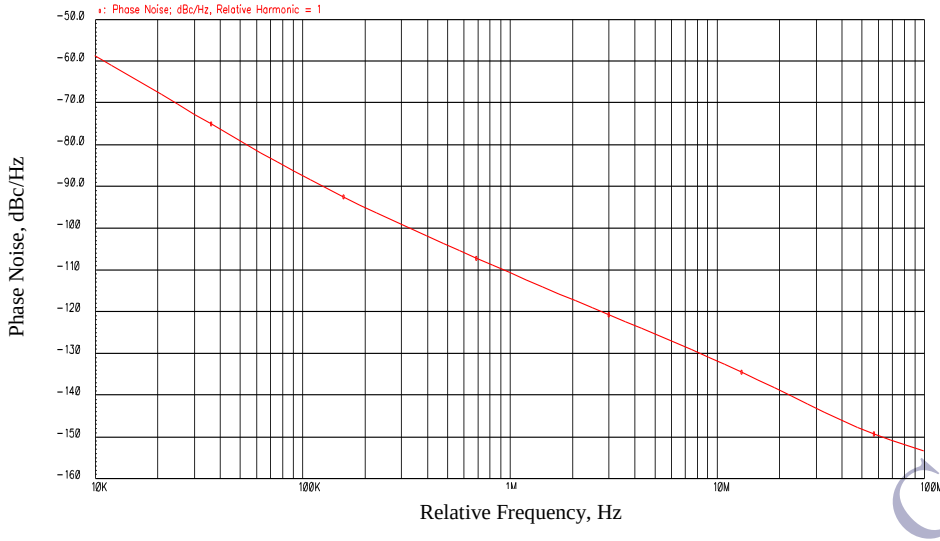


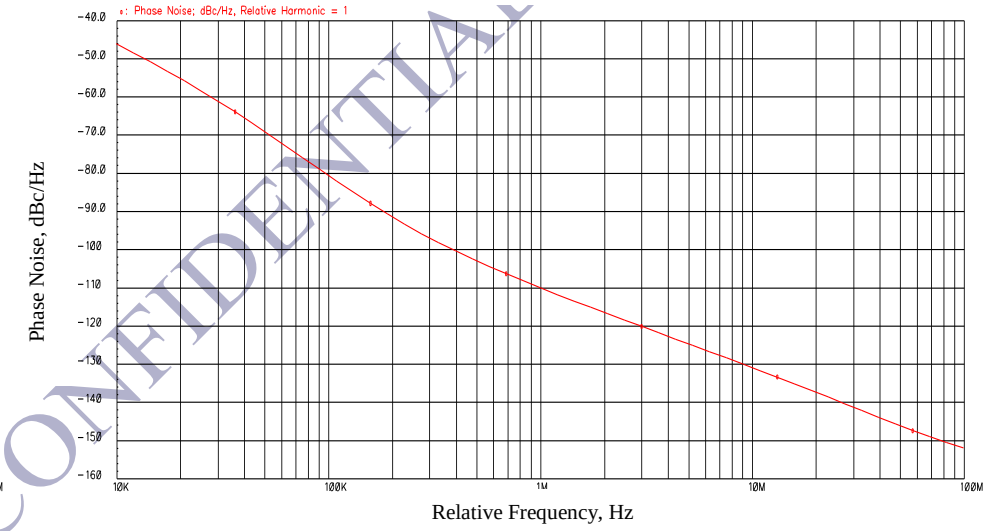
Figure 5. PMCC_VCOMB12G Output Swing Dependencies on Frequency

Periodic Noise Response

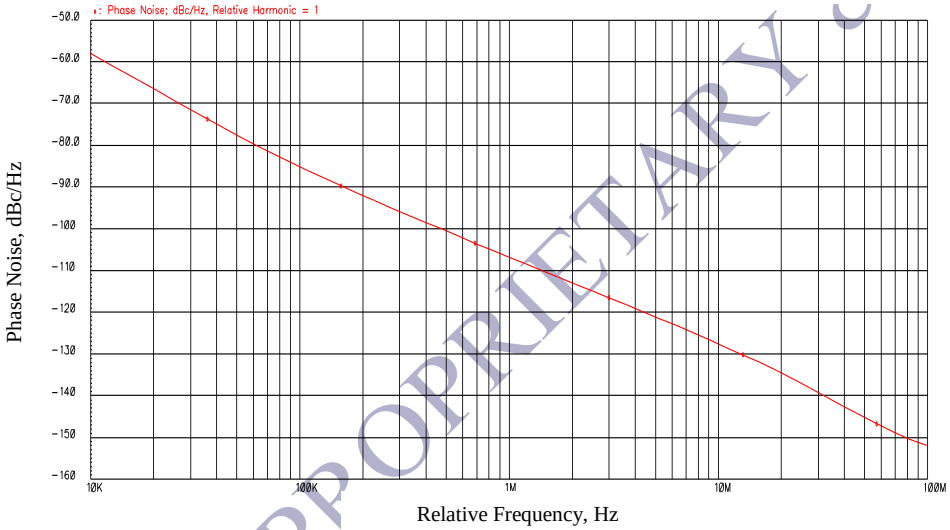
8.5GHz VCO



10.0GHz VCO



10.7GHz VCO



11.1GHz VCO

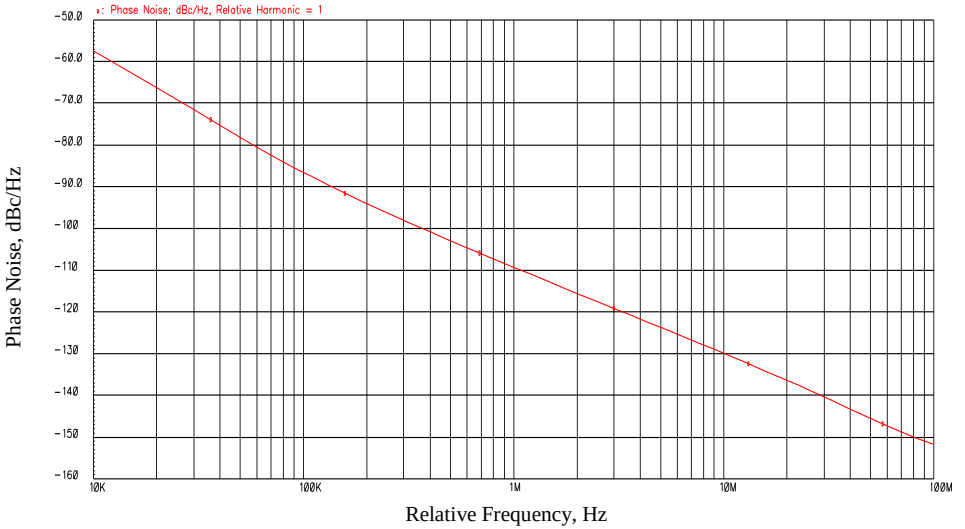


Figure 6. VCO phase noise at nominal corners (Post-Layout, T=25°C).

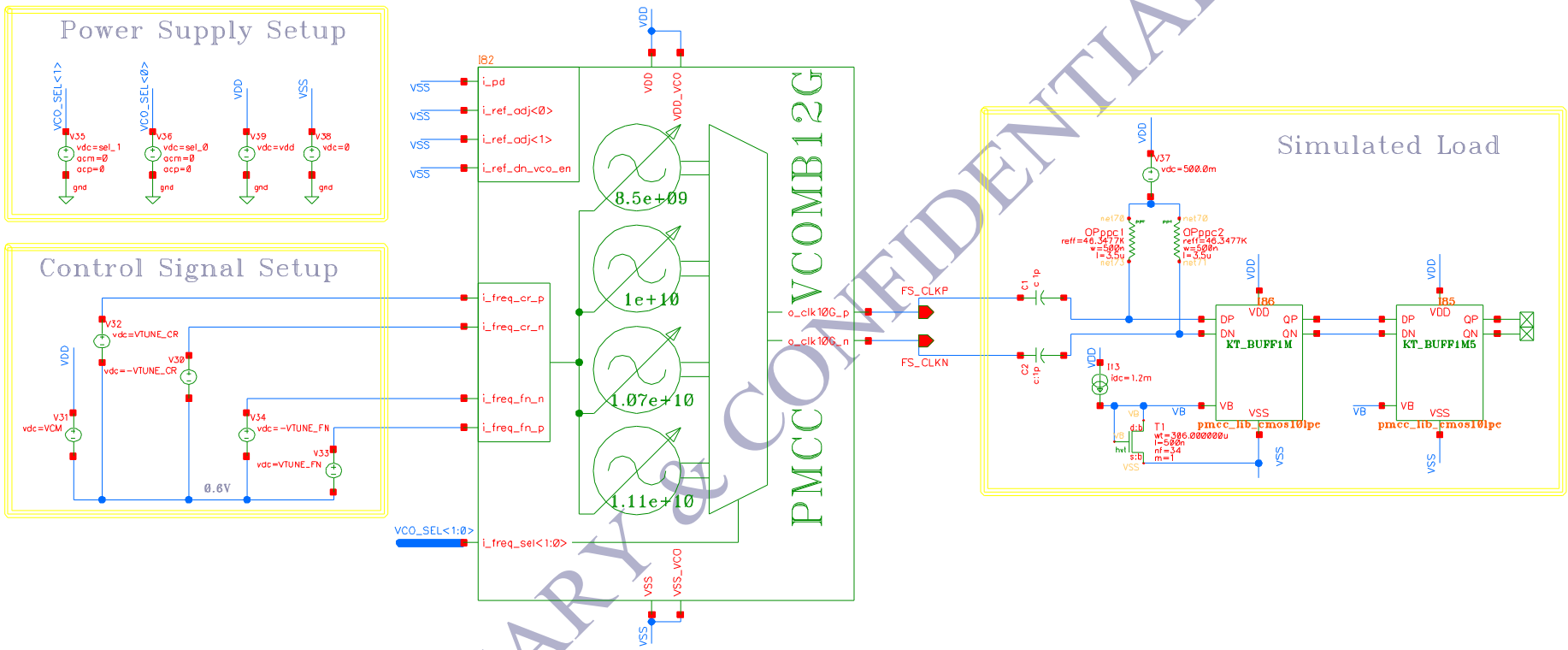


Figure 7. IP block simulation and test schematics

MACRO LAYOUT VIEW

PMCC_VCOMB12G macro layout is optimally designed taking symmetry, parasitic capacitances, inductance and reliability into account. Layout design leverages all 8 metal layers available in the IBM10LPE process 5_01_00_01_LD metal stack. Compact layout ensures minimum parasitic capacitance, inductance, device mismatch and minimum die area.

Layout considerations for macro integration:

- OA is used for ground connections to minimize "ground bounce" effects.
- BA is used for VDD, VDDD, VDD_VCO connection.
- Other layout features incorporated by customer into or adjacent to macro can affect macro performance and should be carefully analyzed.
- Upon request, PMCC can provide IP for different metal stack, can change the macro block shape or migrate the macro block to different process.

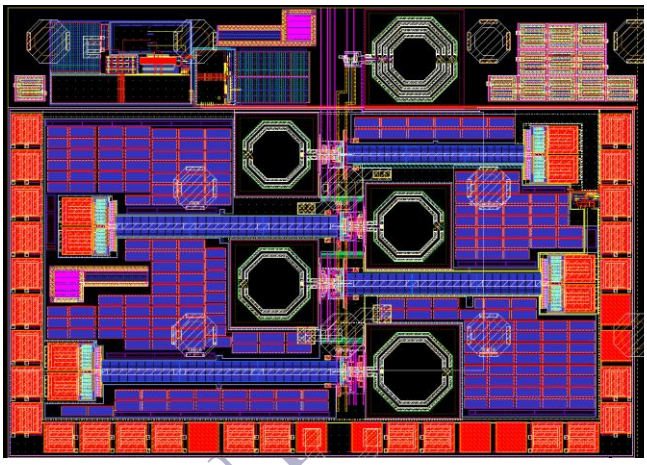


Figure 8. PMCC_VCOMB12G IP macro layout view. Some of the details and/or layers might be omitted. Layout size is 1105µm x 765µm.

Table 5. Version Control

Revision	Date	Author	Changes
V1.0	04/30/10	PMCC	Initial version of the document
V1.1	05/05/10	PMCC	Added simulated fine tuning range. Added Vout (f). Corrected Kvco.
V.1.2	05/18/10	PMCC	Added simulated phase noise.