20-30GHz VCOs

PMCC_VCO20G/24G/25G/26G/30G

IP MACRO **Datasheet Rev 2.4**

Process: Jazz Semiconductor SBC18HX

DESCRIPTION

The PMCC_VCO20G /24G /25G /26G /30G is a set of fully differential high speed VCOs covering 20GHz … 30GHz frequency range, designed using Jazz SiGe120 (SBC18HX) process. Differential architecture ensures substrate and power supply noise immunity. Macro features optional 50 Ohm terminated buffers at its output. Built-in power-down mode enables power saving in case when block is not operated. Operation frequencies, I/O signal levels, control functions and features can be customized upon special agreement.

Applications:

- Frequency Synthesizers
- VSAT Radio
- Point-to-Point/Multi-point Radio
- Test Equipment & Industrial Controls
- Military End-Use
- Automotive Radar
- 100Gb Ethernet

FEATURES

- Center frequency (GHz): 20, 24, 25, 26, 30
- Tuning range: 10%
- Tuning voltage input: 0 … +3.3V
- Phase noise: -105dBc @ 1MHz offset
- Supply voltage: 3.3V ±5%
- Power consumption: 90mW
- Fully differential architecture
- Layout area: 220 x 320 um

FUNCTIONAL DESCRIPTION

Block diagram of macro is shown on Figure 1. Voltage on TUNE pin defines VCO core oscillation frequency. VCO output is fed to output driver, isolating active VCO core from driven circuitry. Output driver provides macro output OUTP/OUTN. PWR_DOWN pin controls macro operating mode: active or power-down. Negative temperature coefficient biasing is provided to compensate VCO frequency temperature dependency.

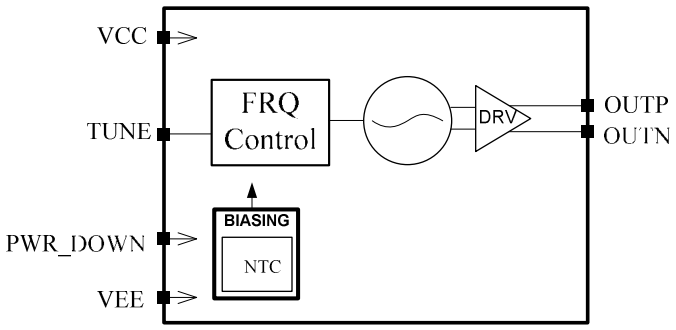

Figure 1. Macro block diagram

MACRO SCHEMATIC SYMBOL. PIN DESCRIPTION

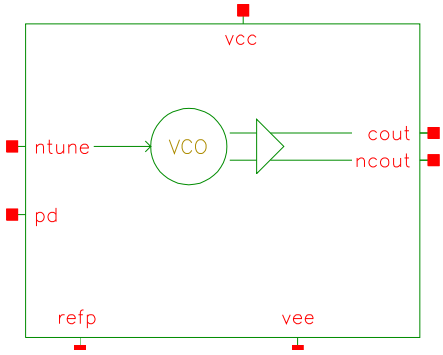

Figure 2. Macro schematic symbol

Pin Name	Description	Type
ntune	Tune voltage	I
cout	VCO CML direct output	O
ncout	VCO CML inverted output	O
vcc	Positive power supply	PWR
vee	Ground	GND
refp	Reference voltage input	I
pd	Power down input	CMOS

AC/DC ELECTRICAL SPECIFICATIONS

Table 1. Absolute maximum ratings

Description	Min	Max	Units
Tune input voltage (pin: ntune)	-0.5	+3.5	V
Power supply (pin vcc)	-0.5	+3.5	V
CMOS control input voltage (pin pd)	-0.5	+3.5	V
Reference voltage input (pin refp)	-0.5	+3.5	V
Junction temperature	-25	125	°C
End Of Life (EOL)	10		years

DC Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. DC Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Positive power supply Vcc		3.1	3.3	3.5	V
Supply current	$T_{junction}$=125°C		27		mA
Supply current in power down state			0.1		mA
NTUNE input voltage Vtune		0		Vcc	V
Power down control input high (Vhi)		1.7		3.5	V
Power down control input low (Vlo)				0.5	V

Table 3. AC Characteristics

Parameter	Min	Typ	Max	Units
Center frequency range *	20		30	GHz
Tuning range *		10		%
Phase Noise @ 1MHz offset		-105		dBc

* Block is subject for optimization for optimum performance at the customer selected frequency within the range provided in the table.

MACRO LAYOUT VIEW

VCO macro layout is optimally designed taking symmetry, parasitic capacitances, inductance and reliability into account. Layout design leverages all 6 metal layers available in the SBC18HXL process. Compact layout ensures minimum parasitic capacitance, inductance, device mismatch and minimum die area.

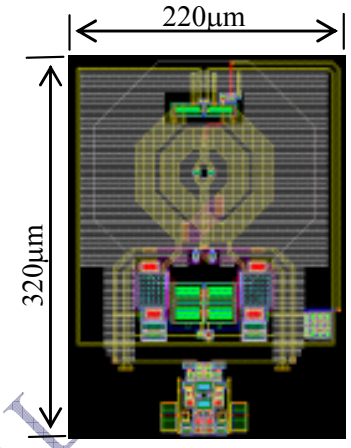

Figure 3. Macro core layout view. Note: some of the details and/or layers might be omitted.

Layout considerations for macro integration:

- METAL6 is used for ground connections to minimize "ground bounce" effects.
- METAL5 is used for VCC connection
- Transmission line structures should be considered for long interconnections in case of macro direct connection to IC pads (through optional 50 Ohm terminated input buffers)
- Other layout features incorporated by customer into or adjacent to macro can affect macro performance and should be carefully analyzed.

IP BLOCK TEST STRUCTURE

Test structure consisting of VCO macro, 50 Ohm terminated output and reference voltage generators is shown on Figure 4. Simulation schematic for test structure is shown on Figure . Test IC layout presented on Figure 6.

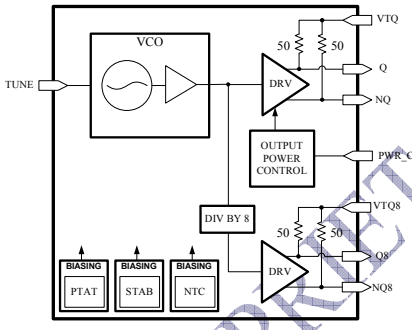

Figure 4. Macro test structure block diagram

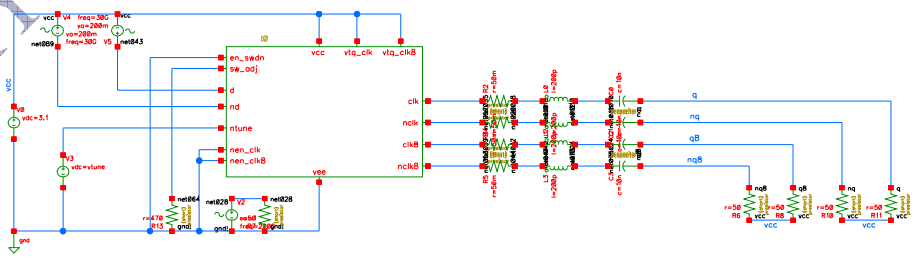

Figure 5. IP block test structure simulation schematic

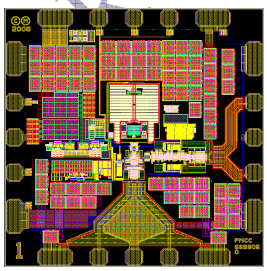

Figure 6. VCO macro test chip layout.