Fractional N PLL 8.5-11.3GHz
PMCC_PLL12GFN

IP MACRO **Datasheet Rev 1**

Process: 65nm CMOS

DESCRIPTION

PMCC_PLL12GFN is a macro-block designed for synthesizing the frequencies required for fiber optic transceivers and serdes using convenient reference frequencies. Fractional N divider is implemented for support of different clocking modes: 79:85, 85:79 (FEC+G.709) 14:15, 15:14 (FEC only) 237:239, 239:237 (G.709 only) 255:239, 239:255 (add FEC to G709 frame). The PLL except ΣΔ modulator is implemented based on differential CML logic for robust operation under strong noise coupling through power, ground and substrate. All biasing currents are programmable within +/-30% for operational margin estimation. Layout is designed using IBM CMOS10LPE 5_01_00_01_LD metal stack. Control functions and layout configuration can be customized upon special agreement.

FEATURES

- Clock monitor output
- Stand-by mode
- 1.2V Power Supply
- Adjustable (+/-30%) reference current
- LOL detection

APPLICATIONS

- SONET/SDH OC-192 transmitter PHY
- 10Ge transmitter with serializer
- 10G back planes
- XFI transmitter with serialization (both line and host side)

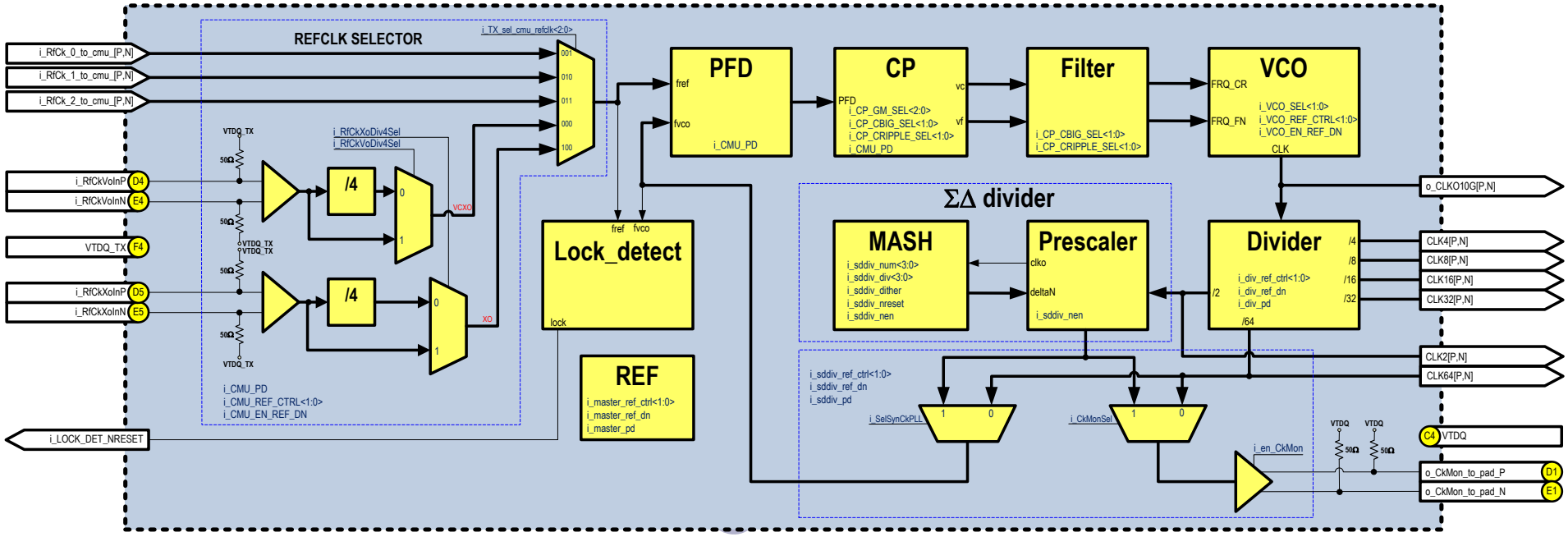

Figure 1. PMCC_PLL_CMU. PLL with CMU Block Diagram

Table 1. Pin Descriptions

Name	Pin #	Description	Type
CLK16N		Base clock output divided by 16. Inverted polarity	AO
CLK16P		Base clock output divided by 16. Direct polarity	AO
CLK2N		Base clock output divided by 2. Inverted polarity	AO
CLK2P		Base clock output divided by 2. Direct polarity	AO
CLK32N		Base clock output divided by 32. Inverted polarity	AO
CLK32P		Base clock output divided by 32. Direct polarity	AO
CLK4N		Base clock output divided by 4. Inverted polarity	AO
CLK4P		Base clock output divided by 4. Direct polarity	AO
CLK64N		Base clock output divided by 64. Inverted polarity	AO
CLK64P		Base clock output divided by 64. Direct polarity	AO
CLK8N		Base clock output divided by 8. Inverted polarity	AO
CLK8P		Base clock output divided by 8. Direct polarity	AO
i_CkMonSel		Clock monitor output selector (0=/64 reference, 1= Sigma-Delta reference)	DI
i_CMU_EN_REF_DN		Biasing power down for CMU	DI
i_CMU_PD		CMU power down	DI
i_CMU_REF_CTRL<1:0>		CMU biasing current adjustment	DI
i_cmuSelRfCk<2:0>		Reference clock selection signal	DI
i_CP_CBIG_SEL<1:0>		Integrating capacitance selection in PLL CMU	DI
i_CP_CRIPPLE_SEL<1:0>		PLL loop filter ripple capacitor selection	DI
i_CP_GM_SEL<2:0>		Gain control bus for PLL CMU	DI
i_div_pd		Power down of clock frequency Divider	DI
i_div_ref_ctrl<1:0>		Biasing current adjustment for Divider	DI
i_div_ref_dn		Biasing power down for Divider	DI
i_en_CkMon		Enable clock monitor signal output	DI
i_LOCK_DET_NRESET		Input for resetting the lock detector	DI
i_master_pd		Power down of the master current reference and the IP MACRO	DI
i_master_ref_ctrl<1:0>		The master current reference adjustment	DI
i_master_ref_dn		Biasing power down for Current References	DI
i_RfCk_0_to_cmu_N		Internal PLL reference clock #1 input. Inverted polarity	AI
i_RfCk_0_to_cmu_P		Internal PLL reference clock #1 input. Direct polarity	AI
i_RfCk_1_to_cmu_N		Internal PLL reference clock #2 input. Inverted polarity	AI
i_RfCk_1_to_cmu_P		Internal PLL reference clock #2 input. Direct polarity	AI
i_RfCk_2_to_cmu_N		Internal PLL reference clock #3 input. Inverted polarity	AI
i_RfCk_2_to_cmu_P		Internal PLL reference clock #3 input. Direct polarity	AI
i_RfCkVoDiv4Sel		VCXO input clock division ratio (0=/64 reference, 1=/16 reference)	DI
i_RfCkVoInN	E4	External PLL reference clock #1 input routed to bump. 50Ω terminated. Inverted polarity	AI
i_RfCkVoInP	D4	External PLL reference clock #1 input routed to bump. 50Ω terminated. Direct polarity	AI
i_RfCkXoDiv4Sel		XO input clock division ratio (0=/64 reference, 1=/16 reference)	DI
i_RfCkXoInN	E5	External PLL reference clock #2 input routed to bump. 50Ω terminated. Inverted polarity	AI

i_RfCkXoInP	D5	External PLL reference clock #2 input routed to bump. 50Ω terminated. Direct polarity	AI
i_sddiv_dither		Dithering control enable for Sigma-Delta Divider	DI
i_sddiv_div<3:0>		The division ratio setting inputs. Division ratio is set by num/div/32	DI
i_sddiv_num<3:0>			DI
i_sddiv_nen		Sigma-Delta Divider enable	DI
i_sddiv_nreset		Sigma-Delta Divider reset signal	DI
i_sddiv_pd		Power down of Sigma-Delta Divider	DI
i_sddiv_ref_ctrl<1:0>		Biasing current adjustment for Sigma-Delta Divider	DI
i_sddiv_ref_dn		Biasing power down for Sigma-Delta Divider	DI
i_SelSynCkPLL		Reference clock input selection signal (0=/64 reference, 1= Sigma-Delta reference)	DI
i_VCO_EN_REF_DN		Biasing current power down for PLL VCO	DI
i_VCO_REF_CTRL<1:0>		Biasing current adjustment for PLL VCO	DI
i_VCO_SEL<1:0>		Input for selecting the VCO frequency	DI
o_CkMon_to_pad_N	E1	Clock monitor signal routed to output routed to a bump. Inverted polarity	AO
o_CkMon_to_pad_P	D1	Clock monitor signal routed to output routed to a bump. Direct polarity	AO
o_CLKO10GN		Base clock output. Inverted polarity	AO
o_CLKO10GP		Base clock output. Direct polarity	AO
o_LOCK		PLL Lock detector full swing CMOS output. "1" indicates lock	DI
VDD	E3	1.2V analog power supply	PW
VDD_VCO	B2, C3, B3, B4	1.2V analog power supply for VCO	PW
VDDD	E2	1.2V digital power supply	PW
VSS	D3	Common node for analog units	GD
VSS_VCO	C2, A3, B5	Common node for VCO	GD
VSSD	D2	Common node for digital units	GD
VTDQ	C4	Power for 50 Ohm output termination resistors	PW

Note: AI – Analog input, DI – digital input, AO – analog output, DO – digital output, PW – power plus, GD – ground/common

Figure 2. Macro schematic symbol

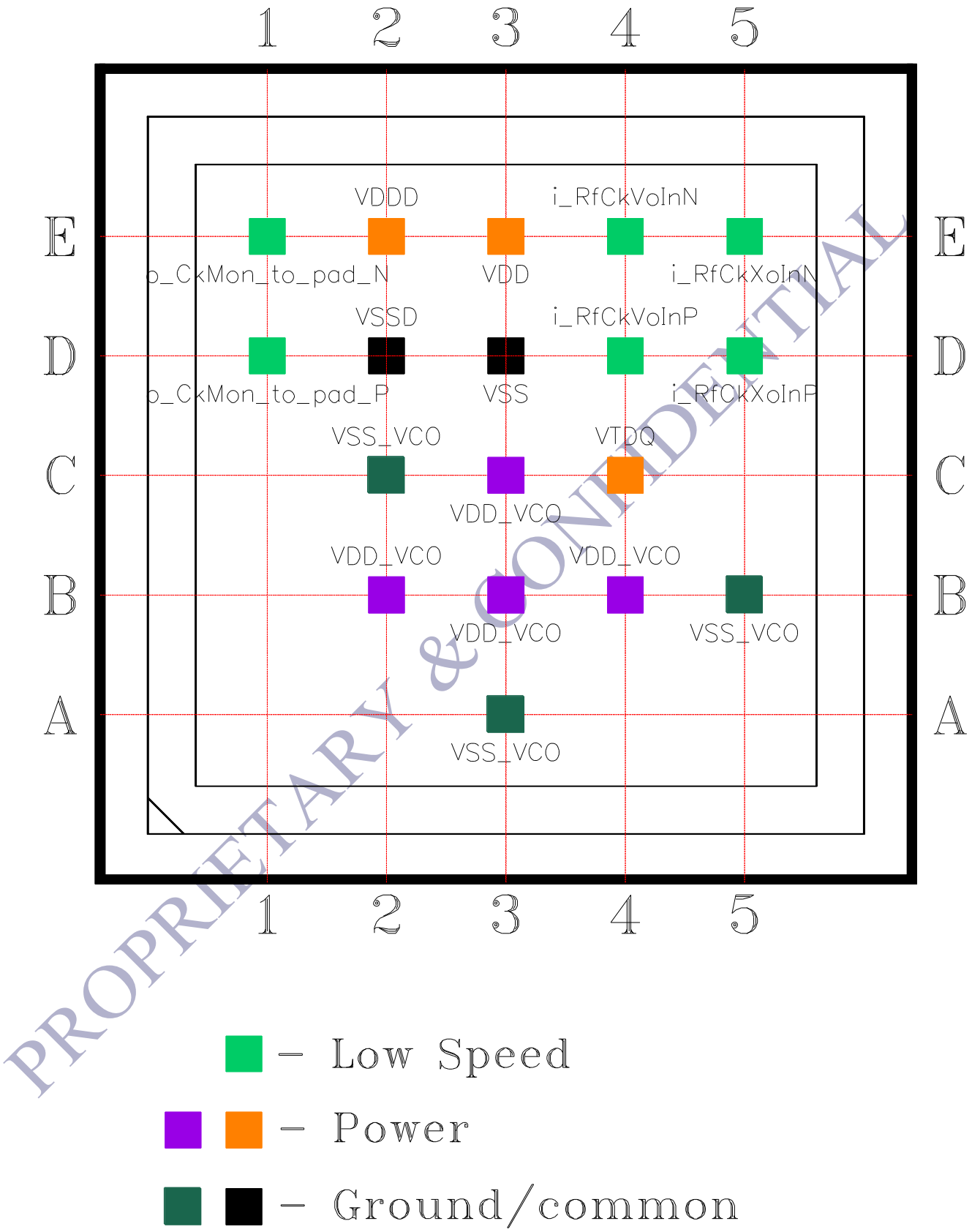

Figure 3. Bump-out diagram

Table 2. Electrical absolute maximum ratings

Description	Min	Max	Units
Power supply VDD	-0.5	1.5	V
Power supply VDDD	-0.5	1.5	V
Power supply VDD_VCO	-0.5	1.5	V
Junction temperature	-55	125	ºC
End Of Life (EOL)	10		years

DC Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes
Power Supply					
Power Supply (VDD)	1.14	1.20	1.26	V	
Power Supply (VDDD)	1.08	1.20	1.32	V	
Power Supply (VDD_VCO)	1.14	1.20	1.26	V	
Power Supply Current		50		mA	
Termination Resistance at the Input (SE)	43	50	59	Ω	Limited by process variation over $\pm 3\sigma$
Termination Resistance at the Output (SE)	43	50	59	Ω	Limited by process variation over $\pm 3\sigma$
Analog core Logic I/O					
Digital input voltage high	0.9	1.2	1.32	V	
Digital input voltage low		0.0	0.32	V	
Digital output voltage high	0.9	1.2	1.32	V	
Digital output voltage low		0.0	0.32	V	
Clock monitors output					
Output swing (single-ended)		400		mVpp	Outputs terminated to 50Ω
Output common mode		1125		mV	

NOTE: Main operation mode.

Table 4. AC Electrical Specifications

I/O Port	Parameter	Symbol	Min.	Typ.	Max.	Units
Clock inputs **i_RfCkVoInP** **i_RfCkVoInN** **i_RfCkXoInP** **i_RfCkXoInN**	**Clock frequency**	F_{CLKX}		$f_b/64$		GHz
	Amplitude	V_{CLKI}		400		mV p-p, SE
	Impedance	R_{CLKI}		50		Ω
Clock inputs **i_RfCk_0_to_cmu_P** **i_RfCk_0_to_cmu_N** **i_RfCk_1_to_cmu_P** **i_RfCk_1_to_cmu_N** **i_RfCk_2_to_cmu_P** **i_RfCk_2_to_cmu_N**	**Clock frequency**	F_{CLKI}		$f_b/64$		GHz
	Amplitude	I_{CLKI}		0.4		mA
	Impedance	R_{CLKI}		1.5		kΩ
Clock outputs **o_CkMon_to_pad_P** **o_CkMon_to_pad_N**	**Clock frequency**		$f_b/16320$		$f_b/16$	GHz
	Impedance (Terminated to VTQ_MON)			50		Ω
	Output swing			250		mV, p-p
	Output common mode			1125		mV
Clock outputs **o_CLKO10GP** **o_CLKO10GN**	**Clock frequency**		8.500	f_b	11.300	GHz
	Impedance			50		Ω
	Output swing			400		mV, p-p, SE
Clock outputs **CLK2P** **CLK2N**	**Clock frequency**		4.250	$f_b/2$	5.650	GHz
	Impedance			274		Ω
	Output swing			400		mV, p-p, SE
Clock outputs **CLK4P** **CLK4N**	**Clock frequency**		2.125	$f_b/4$	2.825	GHz
	Impedance			650		Ω
	Output swing			400		mV, p-p, SE
Clock outputs **CLK8P** **CLK8N**	**Clock frequency**		1.063	$f_b/8$	1.412	GHz
	Impedance			1185		Ω
	Output swing			400		mV, p-p, SE
Clock outputs **CLK16P** **CLK16N**	**Clock frequency**		0.532	$f_b/16$	0.706	GHz
	Impedance			1185		Ω
	Output swing			400		mV, p-p, SE
Clock outputs **CLK32P** **CLK32N**	**Clock frequency**		0.266	$f_b/32$	0.353	GHz
	Impedance			1185		Ω
	Output swing			400		mV, p-p, SE
Clock outputs **CLK64P** **CLK64N**	**Clock frequency**		0.133	$f_b/64$	0.176	GHz
	Impedance			1185		Ω
	Output swing			400		mV, p-p, SE

Simulation schematic for the macro block is shown in Figure 4.

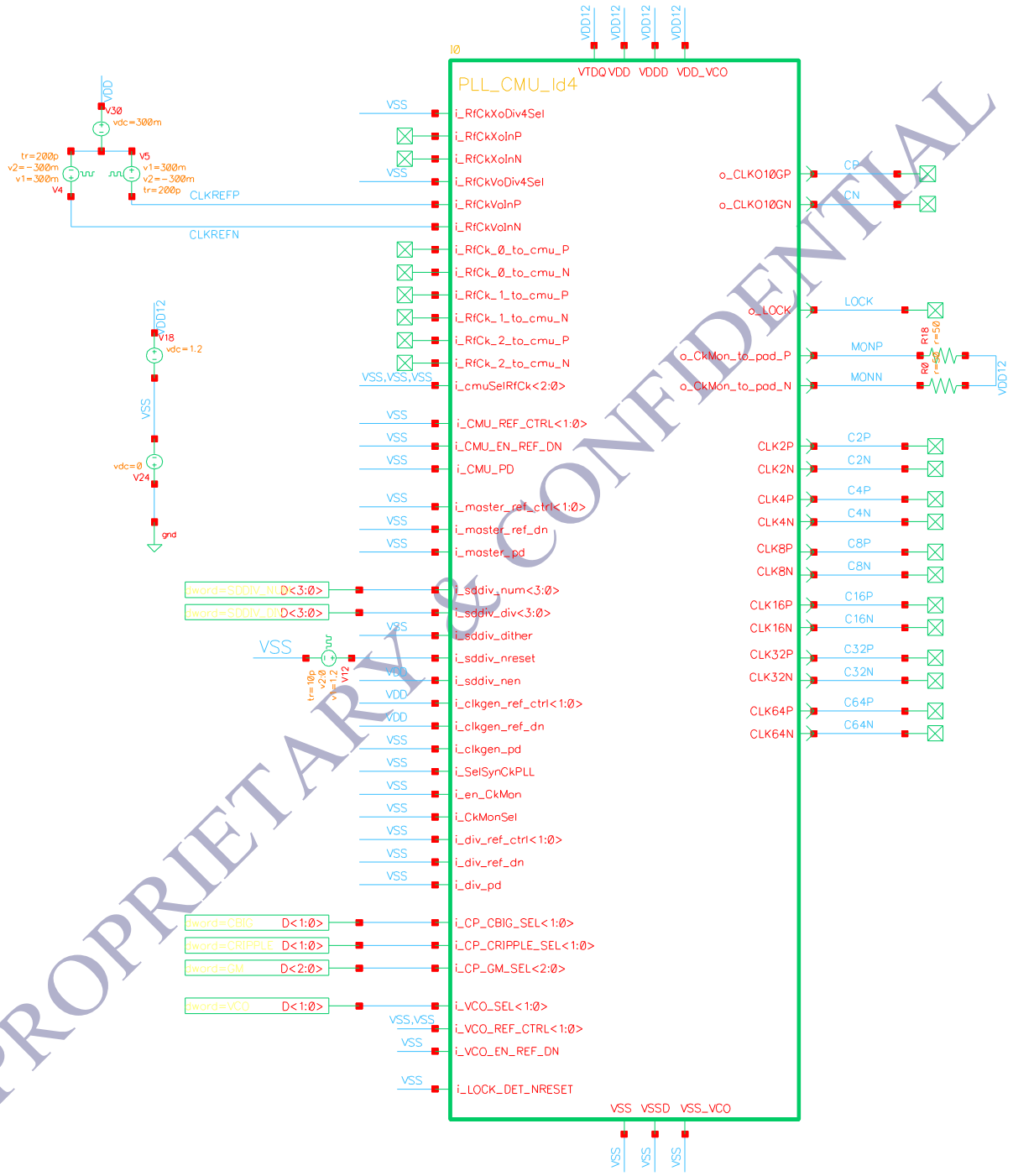

Figure 4. IP block simulation and test schematics

MACRO LAYOUT VIEW

PMCC_PLL12GFN macro layout is optimally designed taking symmetry, parasitic capacitances, inductance and reliability into account. Layout design leverages all 8 metal layers available in the IBM10LPE process 5_01_00_01_LD metal stack. Compact layout ensures minimum parasitic capacitance, inductance, device mismatch and minimum die area.

Layout considerations for macro integration:

- OA is used for ground connections to minimize "ground bounce" effects.
- BA is used for VDD, VDDD, VDD_VCO connection.
- Other layout features incorporated by customer into or adjacent to macro can affect macro performance and should be carefully analyzed.
- Upon request, PMCC can provide IP for different metal stack, can change the macro block shape or migrate the macro block to different process.

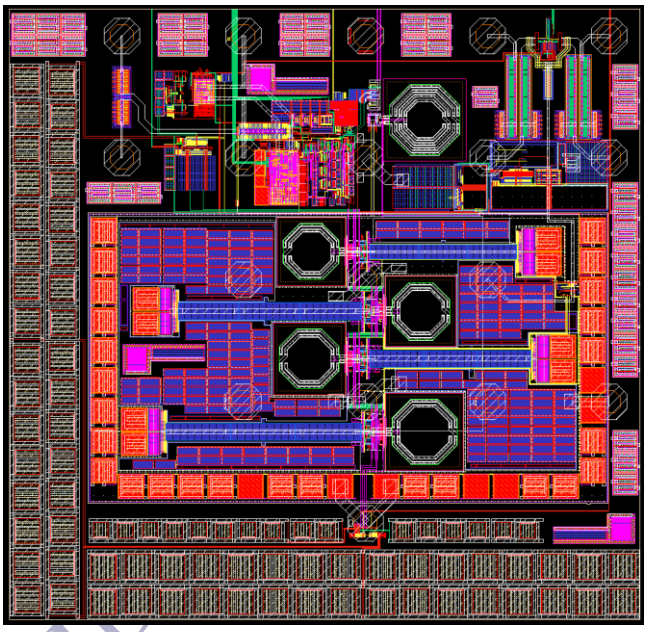

Figure 5. PMCC_PLL_CMU IP macro layout view. Some of the details and/or layers might be omitted. Layout size is 1294µm x 1252µm.

Table 5. Version Control

Revision	Date	Author	Changes
V1.0	04/19/10	PMCC	Initial version of the document