# EA/MZ Modulator Driver
# PMCC_EAMD12G

**IP MACRO** **Datasheet Rev 1.0**

Process: Jazz Semiconductor SBC18HX

## DESCRIPTION

The PMCC_EAMD12G is designed to directly drive the 50Ω inputs of EA or MZ Modulators or EML devices at data-rates up-to 11.3Gbps. The driver features programmable output voltage swing as well as monitoring, crossing point control, and programmable output DC offset (bias). The IP block is designed using Jazz SiGe120 (SBC18HX) process. Modulator driver features fully differential architecture. I/O signal levels, control functions and features can be customized upon special agreement.

Applications include: Electro Absorption and MZ Modulators and DFB lasers in Fiber optic communications; broadband high output swing Limiting Amplifiers from DC to 12Gb/s.

## FEATURES

- Data-rates from 1.25Gb/s to 11.3Gb/s.
- Single –5.2V Power Supply
- Programmable output voltage from 1Vp-p to 3Vp-p Single ended and from 2Vp-p to 6Vp-p differential
- Programmable EAM bias voltage up to 1V
- Crossing point control
- Selectable data retiming
- 90deg at 11.3Gb/s clock phase stepping
- 25ps typical rise/fall-time
- Data polarity invert
- Output Level Monitoring
- Selectable NRZM encoding
- Power consumption: 1W

## BLOCK DIAGRAM

Block diagram of the macro is shown on Figure 1. NRZ data is supplied to the inputs INP/INN. Output data is picked up from outputs OUTP/OUTN. Optional clock is applied to inputs CLKP/CLKN.

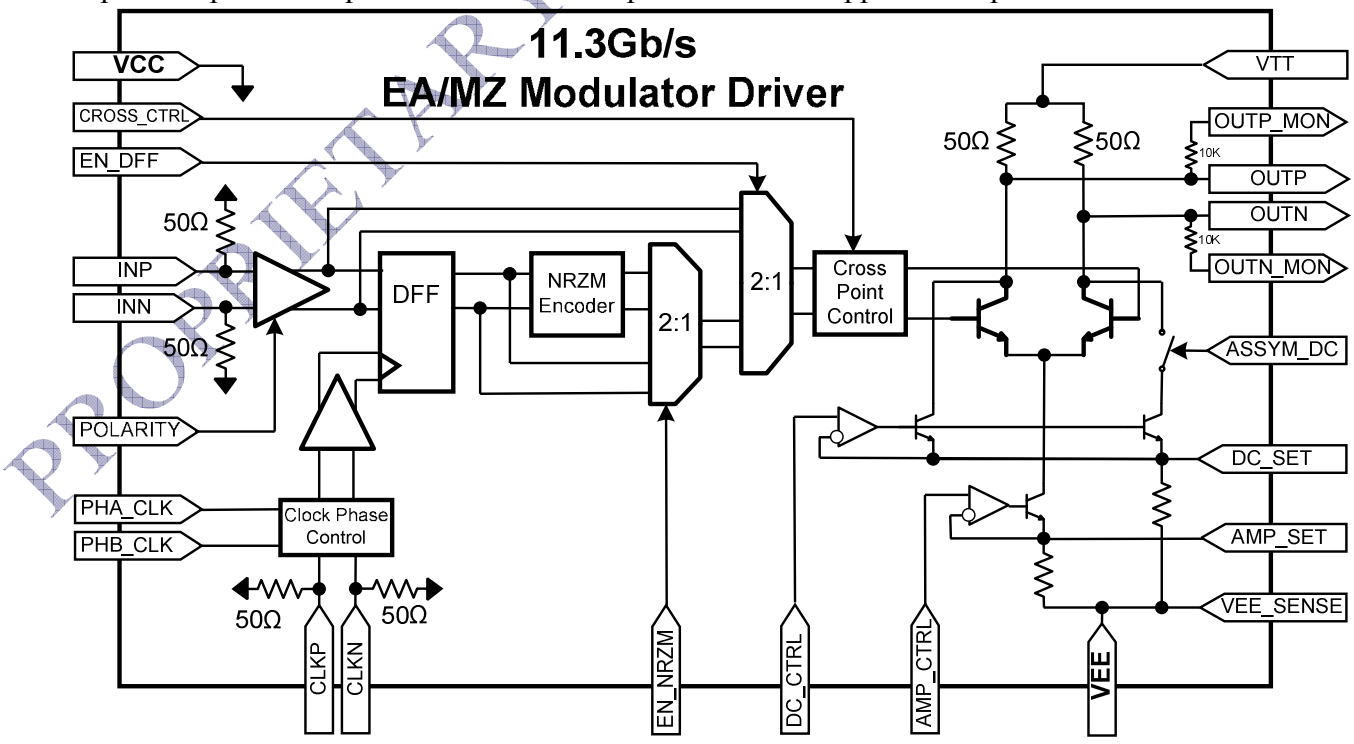


**Figure 1. EA Modulator Driver IP Block Diagram**

MACRO SCHEMATIC SYMBOL. PIN DESCRIPTION.
Table 1 Pin Descriptions

| Name | Pin # | Description | Function |
|---|---|---|---|
| AMP_CTRL | 1 | Control input to vary the driver output swing. Adjusts the $V_{OUT-LOW}$ level with respect to $V_{OUT-HIGH}$ on the OUTP and OUTN outputs. | Analog input |
| DC_CTRL | 2 | Control input to vary the DC bias of the driver output. Simultaneously adjusts $V_{OUT-LOW}$ and $V_{OUT-HIGH}$ on the OUTP and OUTN outputs. | Analog input |
| EN_DFF | 3 | Enables the retiming function. Connect to VCC to enable the retiming on incoming data. Connect to VEE to disable re-timing. | Digital input |
| PHA_CLK | 4 | Controls the phase of the clock. Connect to VCC to enable phase A. Connect to VEE to disable. Look at the truth table of the clock phase select for more details. | Digital input |
| PHB_CLK | 5 | Controls the phase of the clock. Connect to VCC to enable phase B. Connect to VEE to disable. Look at the truth table of the clock phase select for more details. | Digital input |
| CROSS_CTRL | 6 | Controls the cross point of the output data eye. Increasing of the voltage shifts up the crossing point of the output data eye on direct output. Look at the graphs for more information. | Analog input |
| VEE_SENSE | 7,10, 21 | The output is provided for the loopback of control signals. Using of the pin instead of the global ground helps to avoid unwanted ground bounce effects. | VEE |
| AMP_SET | 8 | Sets the initial amplitude of OUTP and OUTN outputs. Connect via 1.8 Ω resistor to VEE_SENSE. See application schematic for details. | Analog input |
| EN_NRZM | 9 | Enables Non-Return-to-Zero-Mark encoding. This function is used as part of optical duo binary encoding. Connect to VCC to enable or to VEE to disable. | Digital input |
| VCC | 11,13, 14,16, 22,24, 26,30, 32,34 | Connect to ground if negative power supply is used (preferred). Connect to VCC if positive power supply is used. | Power supply |
| OUTP OUTN | 12/15 | High-speed differential driver outputs. On-chip 50Ω termination to VTT provided. Each output must be coupled to a 50Ω load. No DC block is allowed. | High speed CML output |
| VTT | 17 | Back Termination for OUTP and OUTN outputs. This pin should be decoupled to ground. See application schematic for details. | Analog |
| OUTN_MON OUTP_MON | 18/19 | Driver output level monitor ports. Connected to the OUTP and OUTN outputs via internal 10KΩ resistors. Connect to VCC or leave open if not used. | Analog output |
| DC_SET | 20 | Sets the initial DC bias level for the OUTP and OUTN outputs. | Analog input |

| | | | |
|---|---|---|---|
| | | Connect via 2.7Ω resistor to VEE_SENSE. See application schematic for details. | |
| CLKP<br>CLKN | 25/23 | High-speed differential clock inputs. On-chip 50Ω termination to VCC provided. Each output must be coupled to a 50Ω load. DC blocking capacitor is needed. See application schematic for details. | High speed Analog input |
| POLARITY | 27 | Data output logic invert.<br>- LOW (or leave open) for normal logic.<br>- HIGH to invert OUTP and OUTN logic. | Digital input |
| VEE | 28,35 | Power supply input. Connect to filtered –5.2V supply. See application schematic for regulation and filter recommendations. Connect to ground if positive power supply is used. | Power supply |
| ASYMM_DC | 29 | Enables asymmetric DC biasing of the differential output.<br>- LOW (or leave open) for normal biasing<br>- HIGH to remove biasing from OUTN | Digital input |
| INP<br>INN | 31/33 | High-speed data differential input. On-chip 50Ω termination to VCC is provided. Each output must be coupled to a 50Ω load. Either DC or AC coupling is allowed. | High speed CML output |
| CB_MON | 36 | A monitoring pin for design validation purposes. Must be left open. | Analog output |

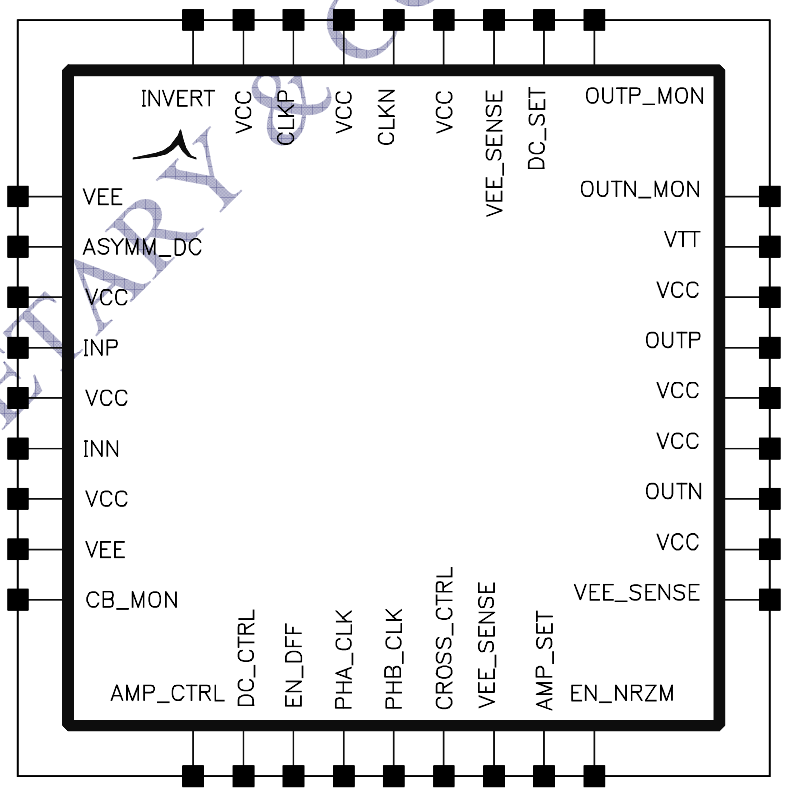


**Figure 2. Macro schematic symbol**

**Table 2. Electrical absolute maximum ratings**

| Description | Min | Max | Units |
|---|---|---|---|
| Power supply (pin VEE) | -6 | | V |
| Control input voltage | -6 | +0.5 | V |
| Junction temperature | -25 | 125 | ºC |
| End Of Life (EOL) | 10 | | years |

*DC Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Table 3. DC Electrical Specifications**

| Parameter | | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Power Supply (VEE) | | -5.46 | -5.2 | -4.95 | V | |
| Power Supply Current | With Retiming Option | | 0.23 | | A | $V_{DC} = 1V, V_{SW} = 2V$ |
| | Without Retiming Option | | 0.22 | | A | $V_{DC} = 1V, V_{SW} = 2V$ |
| | With Retiming Option and 0V DC offset | | 0.2 | | A | $V_{DC}=0V, V_{SW}=3V$ |
| Termination Resistance at the Input (SE) | | 43 | 50 | 59 | Ω | Limits for process variation over $\pm 3\sigma$ |
| Bias Voltage Control Range | | 0 | | 1 | V | Photocurrent from modulator is not accounted for |
| Swing Control Range | | 0.75 | | 3 | V | Photocurrent from Modulator is not taken into account |
| Bias Setting Resistor | | | 2.7 | | Ω | External |
| Swing Setting Resistor | | | 1.8 | | Ω | External |
| Bias Control Voltage (DC_CTRL) | | VEE | | VEE+2 | V | |
| Swing Control Voltage (SWING_CTRL) | | VEE | | VEE+2 | V | |
| Digital Control Input Voltages | Logic High | -1 | | 0 | V | |
| | Logic Low | VEE | | VEE+1 | V | Left open sets logic Low |

**Table 4 AC Electrical Specifications**

| I/O Port | Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | **Data rate** | $f_b$ | 0.155 | 10 | 11.3 | Gb/s |
| | **Programmable Amplitude Range** Single-ended measured into 50Ω, DC offset = 0V, controlled via AMP_ADJ | $V_{OUT}$ | 1.0 | | 3.0 | Vpp |
| | **High Level** varied via DC_ADJ input | $V_{OUT-HIGH}$ | -1.0 | | 0 | V |
| | **Low Level** varied via DC_ADJ & AMP_ADJ | $V_{OUT-LOW}$ | -3.0 | | -1.0 | V |
| | **Rise / Fall Time** Measured at 20% - 80% voltage levels. | $t_r$, $t_f$ | | 25 | 35 | ps |

| I/O Port | Parameter | | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | **Crossing Point Control Range**<br>varied via CPC input | | CPC | 20 | | 80 | % |
| | **Impedance**<br>Terminated to VTT | | $R_{DOUT}$ | | 50 | | Ω |
| | **Return Loss**<br>50MHz – 10GHz | | $S_{22}$ | | | -10 | dB |
| Clock inputs<br><br>**CLKP**<br>**CLKN** | **Clock frequency** | | $F_{CLKO}$ | 0.155 | 10 | 11.3 | GHz |
| | **Amplitude**<br>Single-ended measured into 50Ω. | | $V_{CLKO}$ | 50 | 500 | 1000 | $mV_{pp}$ |
| | **Impedance**<br>Terminated to VCC. | | | | 50 | | Ω |
| | **Return Loss**<br>9GHz – 10GHz | | $S_{11}$ | | | -10 | dB |
| Data inputs<br><br>**INP**<br>**INN** | **Parameter** | | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** |
| | **Data rate** | | $f_b$ | 0.155 | 10 | 11.3 | Gb/s |
| | **Impedance**<br>Terminated to VCC | | $R_{DIN}$ | | 50 | | Ω |
| | Return Loss | | S11 | | | -10 | dB |
| | Input amplitude (single-ended) | Retiming mode | $V_{DR}$ | 30 | | 1500 | $mV_{p-p}$ |
| | | LA mode | $V_D$ | 50 | | 1000 | $mV_{p-p}$ |

## IP BLOCK TEST STRUCTURE

Test structure consisting of PMCC_EAMD12G macro mapped to a wire bond pad ring is available to make possible to tape-out a test chip for macro evaluation. Simulation schematic for the test structure is shown on Figure 3. Test IC layout presented on Figure 4.

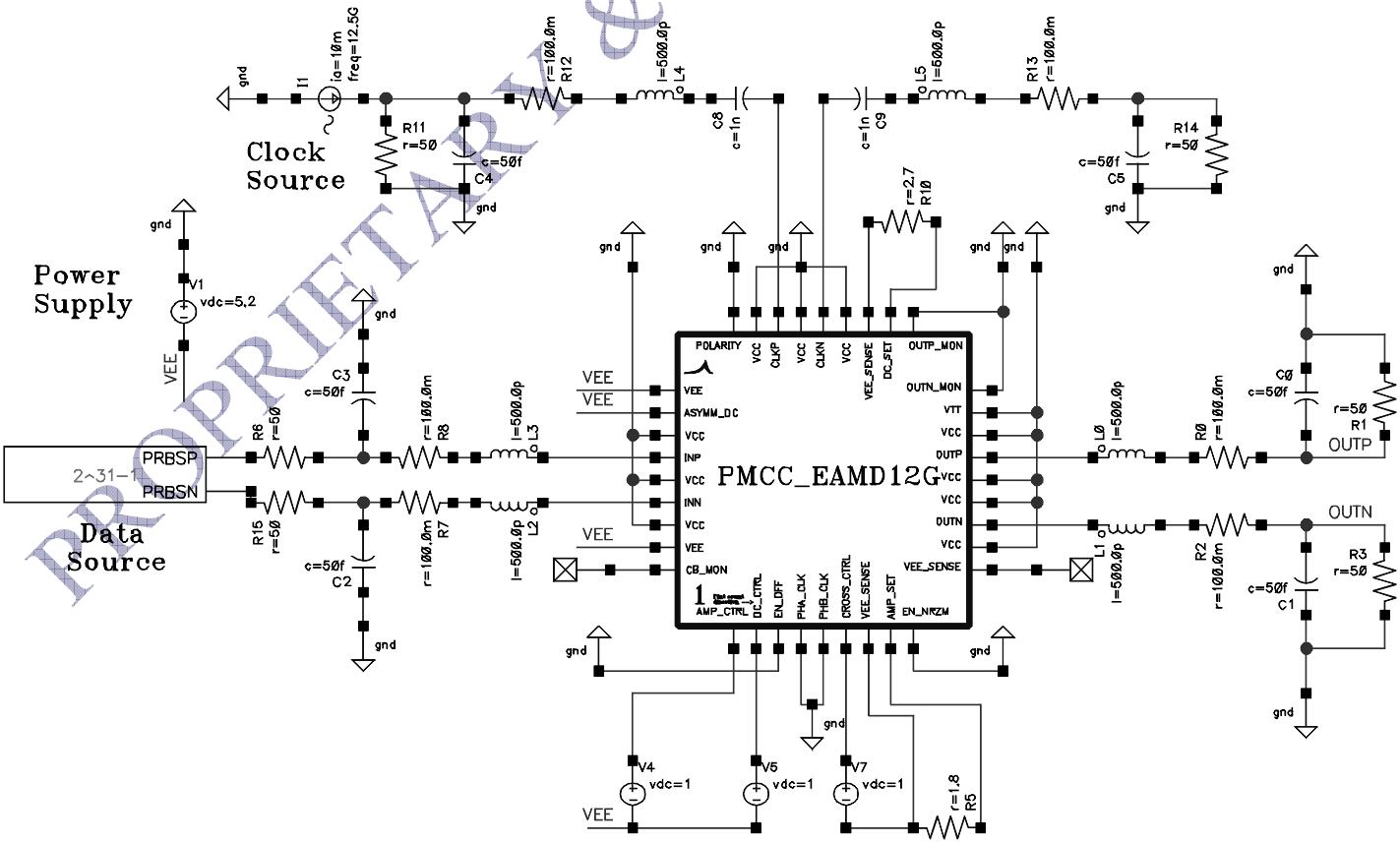


**Figure 3. IP block simulation schematic**

## MACRO LAYOUT VIEW

PMCC_EAMD12G macro layout is optimally designed taking symmetry, parasitic capacitances, inductance and reliability into account. Layout design leverages all 6 metal layers available in the SBC18HX process. Compact layout ensures minimum parasitic capacitance, inductance, device mismatch and minimum die area.

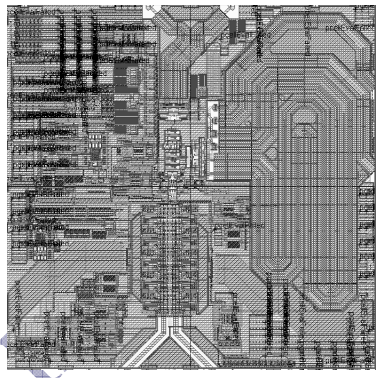

**Figure 4. PMCC_EAMD12G macro core layout view. Note: some of the details and/or layers might be omitted. Layout size is 1270um x 1290um.**

Layout considerations for macro integration:

- METAL6 is used for ground connections to minimize "ground bounce" effects.
- METAL5 is used for VCC connection
- Transmission line structures should be considered for long interconnections in case of macro direct connection to IC pads (through optional 50 Ohm terminated input buffers)
- Other layout features incorporated by customer into or adjacent to macro can affect macro performance and should be carefully analyzed.



**Table 5 Version Control**

| Revision | Date | Author | Changes |
|---|---|---|---|
| V1.0 | 06/18/09 | PMCC | Initial version of the document |
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