60GHz Frequency Divider By 2
PMCC_DIV60G

IP MACRO **Datasheet Rev 2.4**
Process: Jazz Semiconductor SBC18HX

DESCRIPTION

The PMCC_DIV60G is a high speed (up to 60GHz) fully differential static frequency divider by 2, designed using Jazz SiGe120 (SBC18HX) technology. Differential architecture ensures substrate and power supply noise immunity. Macro features input active balun and I/Q outputs with 50 Ohm terminated output drivers (optional). Operation frequencies, I/O signal levels, control functions and features can be customized upon special agreement.

- Phase–locked loop (PLL) applications from DC to 60 GHz
- Point-to-point and point-to-multipoint radios
- Broadband test and measurement equipment
- Radar, electronic warfare, avionics, and space

FEATURES

- Maximum input frequency: 60GHz
- Fully differential 2 latch architecture
- Differential quadrature output
- Input active balun
- Single 3.3V ±5% supply
- Power consumption:
  Core: 180mW
  Active balun: 150mW
- Layout area:
  Core: 120x350 um
  Core + Balun: 300x500 um

FUNCTIONAL DESCRIPTION

Input signal applied to IN_P/IN_N inputs (differentially or single ended) is converted to true differential signal in active balun. Balun differential output is fed to static latch-based frequency divider by 2. Both "I" and "Q" divider outputs are buffered to drive 50 Ohm terminated output buffers (optional).

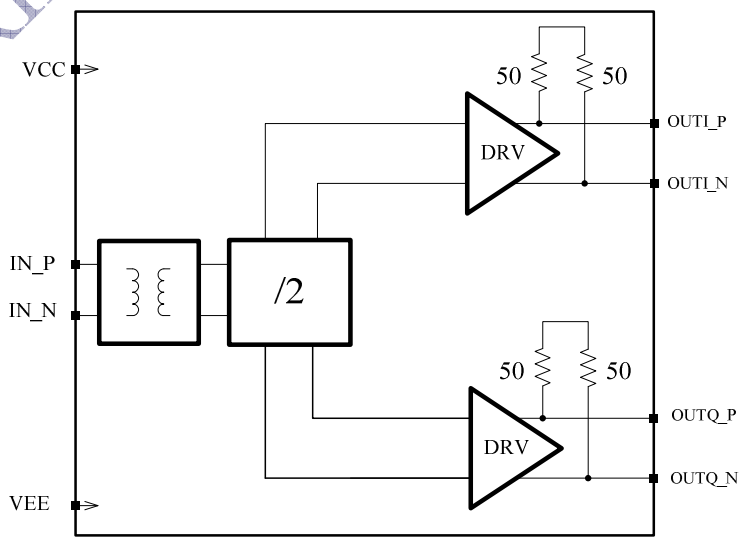
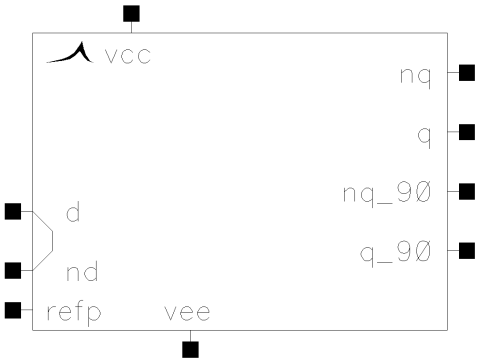


Figure 1. 60GHz static divider macro block diagram

MACRO SCHEMATIC SYMBOL. PIN DESCRIPTION



Pin Name	Description	Type
d	Direct CML input	I
nd	Inverted CML input	I
q	Direct CML output	O
nq	Inverted CML output	O
vcc	Positive power supply	PWR
vee	Ground	GND
refp	Reference voltage input	I

Figure 2. Macro schematic symbol

AC/DC ELECTRICAL SPECIFICATIONS

Table 1. Absolute maximum ratings

Description	Min	Max	Units
Input clock voltage (pins: d,nd)	-0.5	+3.5	V
Power supply (pin vcc)	-0.5	+3.5	V
Reference voltage input (pin refp)	-0.5	+3.5	V
Junction temperature	-25	125	ºC
End Of Life (EOL)	10		years

DC Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. DC Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Positive power supply Vcc		3.1	3.3	3.5	V
Supply current @ Tj=125ºC	+Active Balun +Core		99		mA
	+Active Balun +Core +Output Drivers		200		mA
Input differential swing V_{IN_DIFF}	F_{IN}=60GHz	0.4		1.0	V
Input common mode V_{cm}		Vcc-V_{diff}/2			

Table 3. AC Characteristics

Parameter	Min	Typ	Max	Units
Input frequency*			60	GHz

* Block is subject for optimization for optimum performance at the customer selected frequency within the range as in the table.

MACRO LAYOUT VIEW

Divider macro layout is optimally designed taking symmetry, parasitic capacitances, inductance and reliability into account. Layout utilizes all 6 metal layers available in the SBC18HX process. Compact layout ensures minimum parasitic capacitance, inductance and device mismatch.

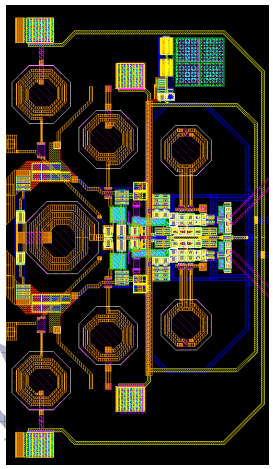


Figure 3. Macro core layout view. Note: some of the details and/or layers might be omitted.

Layout considerations for macro integration:

- METAL6 is used for ground connections to minimize "ground bounce" effects.
- METAL5 is used for VCC connection
- Transmission line structures should be considered for long interconnections in case of macro direct connection to IC pads
- Other layout features incorporated by customer into or adjacent to macro can affect macro performance and should be carefully analyzed.

IP BLOCK TEST STRUCTURE

Test structure consisting of divider macro, 50 Ohm terminated I/Os and reference voltage generators is shown on Figure 4. Divider test IC layout is shown on Figure .

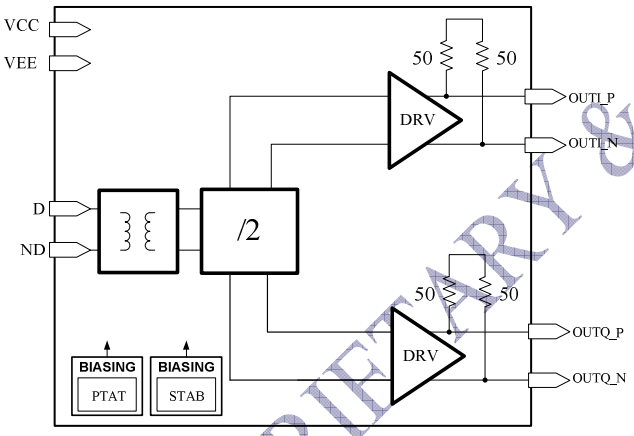


Figure 4. Macro test structure block diagram

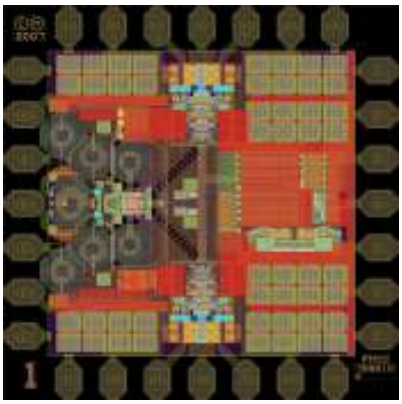


Figure 5. IP block test IC layout