SERDES 1:32 for 8.5-11.3Gb/s PMCC_SERDES12G

Pacific MicroCHIP Corp.

IP MACRO **Datasheet Rev 1.1**

Process: 65nm CMOS

DESCRIPTION

PMCC_SERDES12G is a macro-block consisting of a 32:1 serializer and 1:32 deserializer with supporting functions such as CDR, CMU, loop-backs, LOL, LOS, Equalizer, LA, line rate output driver.

The serdes (except 32 bit I/Os) is implemented based on differential CML logic for robust operation under strong noise coupling through power, ground and substrate.

The data signal in the deserializer is applied to a 50Ω terminated data input is equalized to restore the data eye by the bandwidth limited media such as transmission lines on FR-4 PCBs or coaxial cable. The selectable equalizer can be tuned for the best performance with particular media. An automatic offset control with overriding option (manual or FEC directed) is built in for correcting of duty cycle distorted data such as in fiber optic receivers. The LA following the equalizer is conditioning the data eye for robust CDR operation. CDR phase as well as its dynamics can be adjusted to meet specific jitter tolerance and jitter transfer specifications. Line rate data (8.5-11.3Gb/s) is deserialized to 32-bit parallel data stream and converted to CMOS format for feeding into a FEC or other digital processing block or for feeding out (LVDS output buffers are necessary). LOL and LOS with programmable thresholds are built in for loss of lock and loss of signal indication.
In the serializer the 32 bit wide data stream (CMOS levels) coming from a FEC or another digital block is converted to differential CML levels, serialized and retimed to remove even/odd bit distortion, shape the eye and remove jitter. Serial data is shipped out through a differential 50Ω terminated (each output) data buffer. Multiple dividers (including fractional N) are implemented in the CMU for support of different clocking modes: 79:85, 85:79 (FEC+G.709) 14:15, 15:14 (FEC only) 237:239, 239:237 (G.709 only) 255:239, 239:255 (add FEC to G709 frame). VCXO PLL is included for convenient reference clock generation by using an external high quality oscillator.

All biasing currents are programmable within +/-30% for operational margin estimation in production. DC test points are integrated for measurement of internal temperature, bias voltages and ground potential. Loop backs to/from serializer are integrated for link testing purposes. Layout is designed using IBM CMOS10LPE 5_01_00_01_LD metal stack. Control functions and layout configuration can be customized upon special agreement.

FEATURES

- Data-rates from 8.5Gb/s to 11.3Gb/s.
- High sensitivity input (15mV SE p-p)
- Adjustable input signal equalizer
- Clock and Data Recovery
- Low power consumption (200mW)
- 1.2V and 1.6V Power Supply
- LOS and LOL detection
- Clock synthesizer (including ∑Δ)
- Input and output 50Ω termination
- Adjustable (+/-30%) reference current
- DC test points.
- Integrated temperature sensors
- Manual and automatic offset control
- Stand-by mode
- CDR bandwidth & phase adjustment.
- Line rate loop backs
- Clock monitor output
- Output swing 400mV or 250mV p-p SE
- Output data line rate retiming
- VCXO control PLL

APPLICATIONS

- SONET/SDH OC-192 transceiver with CDR and CMU PHY
- 10GbE serdes transceiver
- 10G back planes
- XFI transceiver with deserialization and serialization (XFP module)

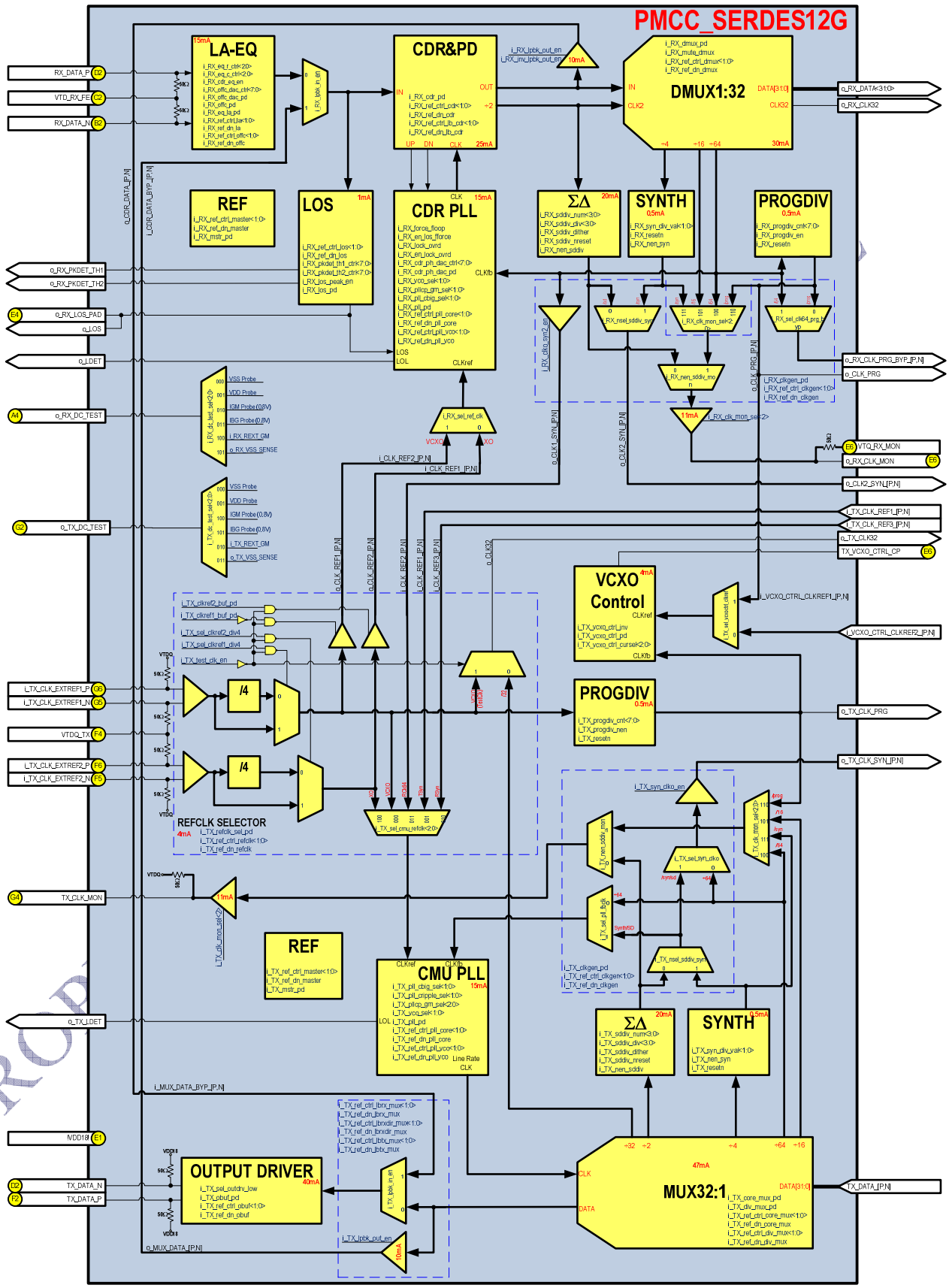

Figure 1. PMCC_SERDES12G. Serializer with CDR and Deserializer with CMU Block Diagram

Table 1 Pin Descriptions

Name	Pin #	Description	Type
Deserializer (PMCC_DSER12G)			
i_RX_ref_ctrl_la<1:0>		The biasing current adjustment for Limiting Amplifier	DI
i_RX_ref_dn_la		The biasing circuit power-down for Limiting Amplifier	DI
i_RX_eq_la_pd		The Equalizer and Limiting Amplifier power-down signal	DI
i_RX_eq_c_ctrl<2:0>		The Equalizer AC response peak frequency selection	DI
i_RX_eq_r_ctrl<2:0>		The Equalizer AC response compensation	DI
i_RX_ref_ctrl_offc<1:0>		The biasing current adjustment for Offset Control	DI
i_RX_ref_dn_offc		The biasing circuit power-down for Offset Control	DI
i_RX_offc_pd		The Offset Control power-down	DI
i_RX_offc_dac_ctrl<7:0>		The Offset Control DAC output current setting	DI
i_RX_offc_dac_pd		The Offset Control DAC power-down	DI
i_RX_cdr_eq_en		Signal spectrum equalization function enable	DI
i_RX_ref_ctrl_los<1:0>		Biasing current adjustment for LOS Detector	DI
i_RX_ref_dn_los		LOS Detector biasing current power-down	DI
i_RX_los_pd		LOS Detector power-down	DI
i_RX_pkdet_th1_ctrl<7:0>		The first threshold level setting for the peak detector	DI
i_RX_pkdet_th2_ctrl<7:0>		The second threshold level setting for the peak detector	DI
i_RX_los_peak_en		Peak detection enable in LOS Detector	DI
i_RX_ref_ctrl_cdr<1:0>		The biasing current adjustment for Clock Data Recovery	DI
i_RX_ref_dn_cdr		The biasing circuit power-down for Clock Data Recovery	DI
i_RX_ref_ctrl_lb_cdr<1:0>		The biasing current adjustment for Loopback circuits	DI
i_RX_ref_dn_lb_cdr		The biasing circuitry power-down for Loopback	DI
i_RX_cdr_pd		The Clock Data Recovery power-down	DI
i_RX_cdr_ph_dac_ctrl<7:0>		CPCDR integrator current setting DAC input	DI
i_RX_cdr_ph_dac_pd		CPCDR integrator current setting DAC power down	DI
i_RX_lpbk_in_en		High state will enable the serial loopback circuitry	DI
i_RX_inv_lpbk_out_en		High state will enable the inversion of the signal in the serial loopback	DI
i_RX_lpbk_out_en		High state will enable the serial loopback circuitry	DI
RX_DATA_P	K2	RX frontend direct line rate data input	AI
RX_DATA_N	I2	RX frontend inverted line rate data input	AI
i_RX_ref_ctrl_dmux<1:0>		The biasing current adjustment for Demultiplexer	DI
i_RX_ref_dn_dmux		The biasing circuitry power-down for Demultiplexer	DI
i_RX_dmux_pd		Demultiplexer power-down	DI
i_RX_mute_dmux		Demultiplexer data output to processing core suspend signal	DI
i_RX_pllcp_gm_sel<1:0>		CPCDR gain selection	DI
i_RX_pll_cbig_sel<1:0>		CPCDR integrating capacitance value selection signal	DI
i_RX_en_los_fforce		Enables the LOS signal to be used in PLL frequency locking loop	DI
i_RX_lock_ovrd		Frequency locking override signal	DI

i_RX_en_lock_ovrd		Frequency locking override signal enable signal	DI
i_RX_vco_sel<1:0>		VCO frequency selection signal	DI
i_RX_ref_ctrl_pll_core<1:0>		PLL biasing current adjustment level control	DI
i_RX_ref_ctrl_pll_vco<1:0>		PLL VCO biasing current adjustment level control	DI
i_RX_ref_dn_pll_core		PLL biasing power-down	DI
i_RX_ref_dn_pll_vco		PLL VCO biasing power-down	DI
i_RX_pll_pd		PLL power-down	DI
i_RX_force_floop		High state will force PLL's loss of lock and assert centering PLL. The lock detector is forced low	DI
i_RX_sel_ref_clk		The reference clock (0=VCXO, 1=XO) selection signal	DI
i_RX_syn_div_val<1:0>		Clock synthesizer clock division ratio	DI
i_RX_nen_syn		Synthesizer disablement signal	DI
i_RX_nsel_sddiv_syn		Clock synthesizer selection for clock generation	DI
i_RX_sddiv_num<3:0>		The division ration setting inputs. Division ratio is set by num/div/32	DI
i_RX_sddiv_div<3:0>			DI
i_RX_sddiv_dither		Dithering control enable for Sigma-Delta Divider	DI
i_RX_nen_sddiv		Sigma-Delta Divider enable	DI
i_RX_sddiv_nreset		Sigma-Delta Divider reset signal	DI
i_RX_progdiv_cnt<7:0>		The signal representing number by which the CLK/16 will be divided by the programmed divider	DI
i_RX_progdiv_en		Programmable Divider enable signal	DI
i_RX_resetn		The master reset of RX internal state	DI
i_RX_ref_ctrl_clkgen<1:0>		The biasing current adjustment for Clock Generator	DI
i_RX_ref_dn_clkgen		The biasing circuitry power-down for Clock Generator	DI
i_RX_clkgen_pd		The Clock Generator power-down	DI
i_RX_clko_syn2_en		High state will enable the direct transfer of the recovered clock eto serializer for line timing	DI
i_RX_clk_mon_sel<2:0>		The receiver clock monitor selector control	DI
i_RX_sel_clk64_prg_byp		High state will enable the clock pass-through	DI
i_RX_nen_sddiv_mon		Sigma-Delta Divider output monitor	DI
i_RX_dc_test_sel<2:0>		Signal for selection of DC Test Point channel	DI
i_RX_ref_ctrl_master<1:0>		The current adjustment of internal reference current sources e	DI
i_RX_ref_dn_master		The power-down of internal reference current sources	DI
i_RX_mstr_pd		The power-down signal for internal reference current sources, CDR and DMUX	DI
i_RX_REXT_GM	I5	GM reference external resistor. Connect 3.5K resistor to this pad	DI
o_RX_VSS_SENSE	I4	RX ground return path for GM reference external resistor	AO
o_RX_LOS_PAD	L4	buffered LOS detector full swing CMOS output routed to a bump. "1" indicates loss of signal	DO
o_RX_LOS		LOS detector full swing CMOS output. "1" indicates loss of signal	DO
o_RX_PKDET_TH1		RX frontend LOS peak detector digital output. "1" indicates input signal above programmable threshold level 1	DO
o_RX_PKDET_TH2		RX frontend LOS peak detector digital output. "1" indicates input signal	DO

		above programmable threshold level 2	
o_RX_DATA<31:0>		Recovered and de-serialized 1:32 data stream full swing CMOS output; retimed and matched with o_CLK32	DO
o_RX_CLK32		Full swing CMOS recovered /32 clock output	DO
o_RX_LDET		CDR PLL Lock detector full swing CMOS output. "1" indicates lock	DO
o_CLK1_SYN_P		Programmable divider direct clock output	AO
o_CLK1_SYN_N		Programmable divider inverted clock output	AO
o_CLK2_SYN_P		#2 clock synthesizer direct output	AO
o_CLK2_SYN_N		#2 clock synthesizer inverted output	AO
o_RX_CLK_PRG		Full swing CMOS programmable divider output	DO
o_RX_CLK_PRG_BYP_P		programmable divider direct clock output with bypass by recovered /64 clock option	AO
o_RX_CLK_PRG_BYP_N		programmable divider inverted clock output with bypass by recovered /64 clock option	AO
o_RX_CLK_MON	H5	Clock monitoring routed to a bump	DO
o_RX_DC_TEST	H4	DC test point output routed to a bump	AO
VTD_RX_FE	J2	1.2V analog power supply for input termination resistors	PW
VTQ_RX_MON	J4	1.2 analog power supply for clock monitoring output termination resistors	PW
VDD	N1, N5, K4, G3, D1,	1.2V analog power supply	PW
VDDD	J5, D4	1.2V digital power supply	PW
VDD_RXVCO	N3, N4, M5, L2	1.2V analog power supply for VCO	PW
VSS	D3, E2, F3, G4, H1, H3, J3, K3, N2	Common node for analog units	GD
VSSD	H3, E4	Common node for digital units	GD
VSS_RXVCO	L2, M5	Common node for VCO	GD
Serializer (PMCC_SER12G)			
i_TX_dc_test_sel<2:0>		Input signal determining the DC Test point channel	DI
i_TX_ref_ctrl_div_mux<1:0>		Biasing current adjustment for Multiplexer's dividers	DI
i_TX_ref_ctrl_lbrxdir_mux<1:0>		Biasing current adjustment for Loopback with RX circuit	DI
i_TX_ref_ctrl_lbrx_mux<1:0>		Biasing current adjustment for Loopback with RX circuit	DI
i_TX_ref_ctrl_lbtx_mux<1:0>		Biasing current adjustment for Loopback with RX CDR circuit	DI
i_TX_ref_ctrl_core_mux<1:0>		Biasing power down for Multiplexer Core	DI
i_TX_ref_dn_div_mux		Biasing power down for Multiplexer Dividers	DI
i_TX_ref_dn_lbrxdir_mux		Biasing power down for Loopback	DI
i_TX_ref_dn_lbrx_mux		Biasing power down for Loopback	DI
i_TX_ref_dn_lbtx_mux		Biasing power down for Loopback	DI
i_TX_ref_dn_core_mux		Biasing power down for Multiplexer Core	DI
i_TX_core_mux_pd		Multiplexer power down	DI
i_TX_div_mux_pd		Power down of clock frequency dividers for multiplexer core	DI
i_TX_lpbk_in_en		Enable signal of loopback between CDR and CMU	DI

i_TX_lpbk_out_en		Enable signal of loopback between CMU and CDR	DI
i_TX_sel_outdrv_low		High state will put CML output buffer in low-swing output mode	DI
i_TX_ref_ctrl_obuf<1:0>		Biasing current adjustment for Output Buffer	DI
i_TX_ref_dn_obuf		Biasing power down for Output Buffer	DI
i_TX_obuf_pd		Power-down of Output Buffer	DI
i_TX_DATA<31:0>		Serializer 32:1 input data stream. Full swing CMOS output	DI
i_VCXO_CTRL_CLKREF2_P		VCXO PLL reference clock input #2. Direct polarity	DI
i_VCXO_CTRL_CLKREF2_N		VCXO PLL reference clock input #2. Inverted polarity	DI
i_TX_sel_vcxoctrl_clkref		Programmable reference clock source selection signal	DI
i_TX_vcxo_ctrl_inv		VCXO reference tuning slope inversion signal	DI
i_TX_vcxo_ctrl_pd		Reference clock controller power down	DI
i_TX_vcxo_ctrl_cursel<2:0>		Biasing current adjustment for VCXO	DI
i_TX_SynDivVal<1:0>		Clock synthesizer clock division ratio	DI
i_TX_nen_syn		Synthesizer disablement signal	DI
i_TX_nsel_sddiv_syn		Clock synthesizer selection for clock generation	DI
i_TX_sddiv_num<3:0>		The division ration setting inputs. Division ratio is set by num/div/32	DI
i_TX_sddiv_div<3:0>			DI
i_TX_sddiv_dither		Dithering control enable for Sigma-Delta Divider	DI
i_TX_nen_sddiv		Sigma-Delta Divider enable	DI
i_TX_nen_sddiv_mon		Sigma-Delta Divider output monitor	DI
i_TX_sddiv_nreset		Sigma-Delta Divider reset signal	DI
i_TX_progdiv_cnt<7:0>		The signal representing number by which the CLK/16 will be divided by the programmed divider	DI
i_TX_progdiv_nen		Programmable Divider disable signal	DI
i_TX_resetn		Input for resetting the internal IP MACRO state	DI
i_TX_ref_ctrl_clkgen<1:0>		The Clock Synthesizer biasing current adjustment	DI
i_TX_ref_dn_clkgen		Biasing power down for Clock Generator	DI
i_TX_clkgen_pd		Clock generator power down	DI
i_TX_syn_clko_en		Enable the output buffer of the clock synthesizer	DI
i_TX_sel_syn_clko		Synthesized reference clock output (0=/64, 1=/synth)	DI
i_TX_sel_pll_fbclk		Reference clock input selection signal (0=/64, 1=/synth)	DI
i_TX_clk_mon_sel<2:0>		The receiver clock monitor selector control	DI
i_TX_pll_cbig_sel<1:0>		Integrating capacitance selection in PLL CMU	DI
i_TX_pll_cripple_sel<1:0>		PLL loop filter ripple capacitor selection	DI
i_TX_pllcp_gm_sel<2:0>		Gain control bus for PLL CMU	DI
i_TX_vco_sel<1:0>		Input for selecting the VCO frequency	DI
i_TX_ref_ctrl_pll_core<1:0>		Biasing current adjustment for PLL core	DI
i_TX_ref_ctrl_pll_vco<1:0>		Biasing current adjustment for PLL VCO	DI
i_TX_ref_dn_pll_core		Biasing current power down for PLL Core	DI
i_TX_ref_dn_pll_vco		Biasing current power down for PLL VCO	DI
i_TX_pll_pd		Power down for PLL	DI

i_TX_CLK_EXTREF2_P	E5	External PLL reference clock #2 input routed to bump. Direct polarity	DI
i_TX_CLK_EXTREF2_N	D5	External PLL reference clock #2 input routed to bump. Inverted polarity	DI
i_TX_CLK_EXTREF1_P	F5	External PLL reference clock #1 input routed to bump. Direct polarity	DI
i_TX_CLK_EXTREF1_N	G5	External PLL reference clock #1 input routed to bump. Inverted polarity	DI
i_TX_CLK_REF1_P		Internal PLL reference clock #1 input. Direct polarity	DI
i_TX_CLK_REF1_N		Internal PLL reference clock #1 input. Inverted polarity	DI
i_TX_CLK_REF3_P		Internal PLL reference clock #3 input. Direct polarity	DI
i_TX_CLK_REF3_N		Internal PLL reference clock #3 input. Inverted polarity	DI
i_TX_clkref2_buf_pd		XO input clock buffer power up	DI
i_TX_clkref1_buf_pd		VCXO output buffer power down	DI
i_TX_sel_clkref1_div4		VCXO input clock division ratio (0=/64 reference, 1=/16 reference)	DI
i_TX_sel_clkref2_div4		XO input clock division ratio (0=/64 reference, 1=/16 reference)	DI
i_TX_test_clk_en		Test clock enable signal	DI
i_TX_sel_cmu_refclk<2:0>		Reference clock selection signal	DI
i_TX_ref_ctrl_refclk<1:0>		The CMU biasing current adjustment	DI
i_TX_ref_dn_refclk		Biasing power down for Clock Selector	DI
i_TX_refclk_sel_pd		Power down of reference clock selector	DI
i_TX_mstr_pd		Power down of all TX current references and the TX circuitry	DI
i_TX_ref_ctrl_master<1:0>		The current reference current adjustment	DI
i_TX_ref_dn_master		Biasing power down for Current References	DI
i_TX_REXT_GM	G1	External resistor bump pad connection	DI
o_TX_DC_TEST	G2	DC Test Point Multiplexer to output routed to a bump	AO
TX_dataP	F2	Line rate serial data output produced by serializer 32:1. Direct output routed to bump	AO
TX_dataN	D2	Line rate serial data output produced by serializer 32:1. Inverted output routed to bump	AO
TX_VCXO_CTRL_CP	B5	VCXO control charge pump output routed to a bump	DO
o_CLK_REF1_P		Internal PLL reference clock #1 input. Direct polarity	DO
o_CLK_REF1_N		Internal PLL reference clock #1 input. Inverted polarity	DO
TX_CLK_MON	G4	Clock monitor signal routed to output routed to a bump	DO
o_TX_CLK_PRG		Full swing CMOS programmable divider output	DO
o_TX_LDET		CDR PLL Lock detector full swing CMOS output. "1" indicates lock	DO
o_TX_CLK32		Full swing CMOS recovered /32 clock output	DO
o_TX_VSS_SENSE	F1	Common node sensing bump pad	AO
VTDQ_TX	F4	Power for 50Ohm output termination resistors	PW
VDD_VCXOCP	A5	1.2V analog power for VCXOCP	PW
VDD1P6	E1	1.6V analog power supply for Output Driver	PW
VDD_TXVCO	B2, B3, B4, C3	1.2V analog power for VCXOCP	PW
VSS_TXVCO	A3, C2, C4	Common node for VCO	GD

Note: AI – Analog input, DI – digital input, AO – analog output, DO – digital output, PW – power plus, GD – ground/common

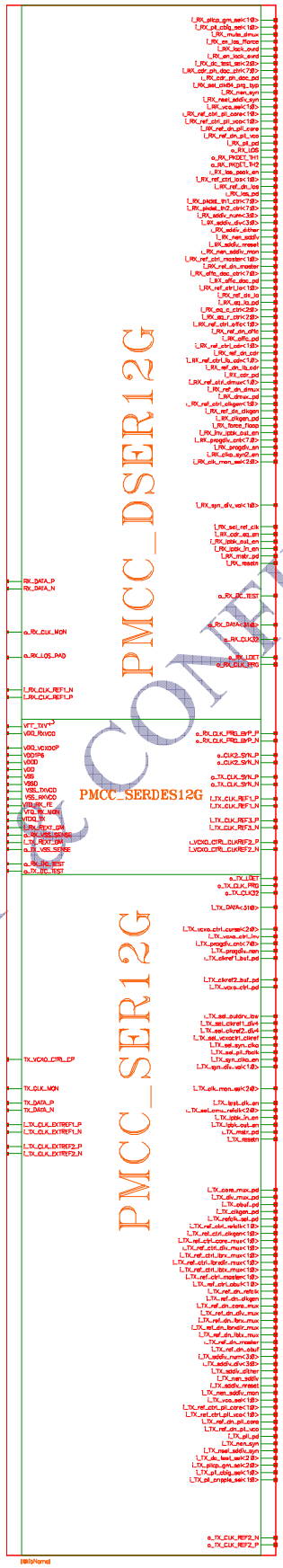

Figure 2. Macro schematic symbol

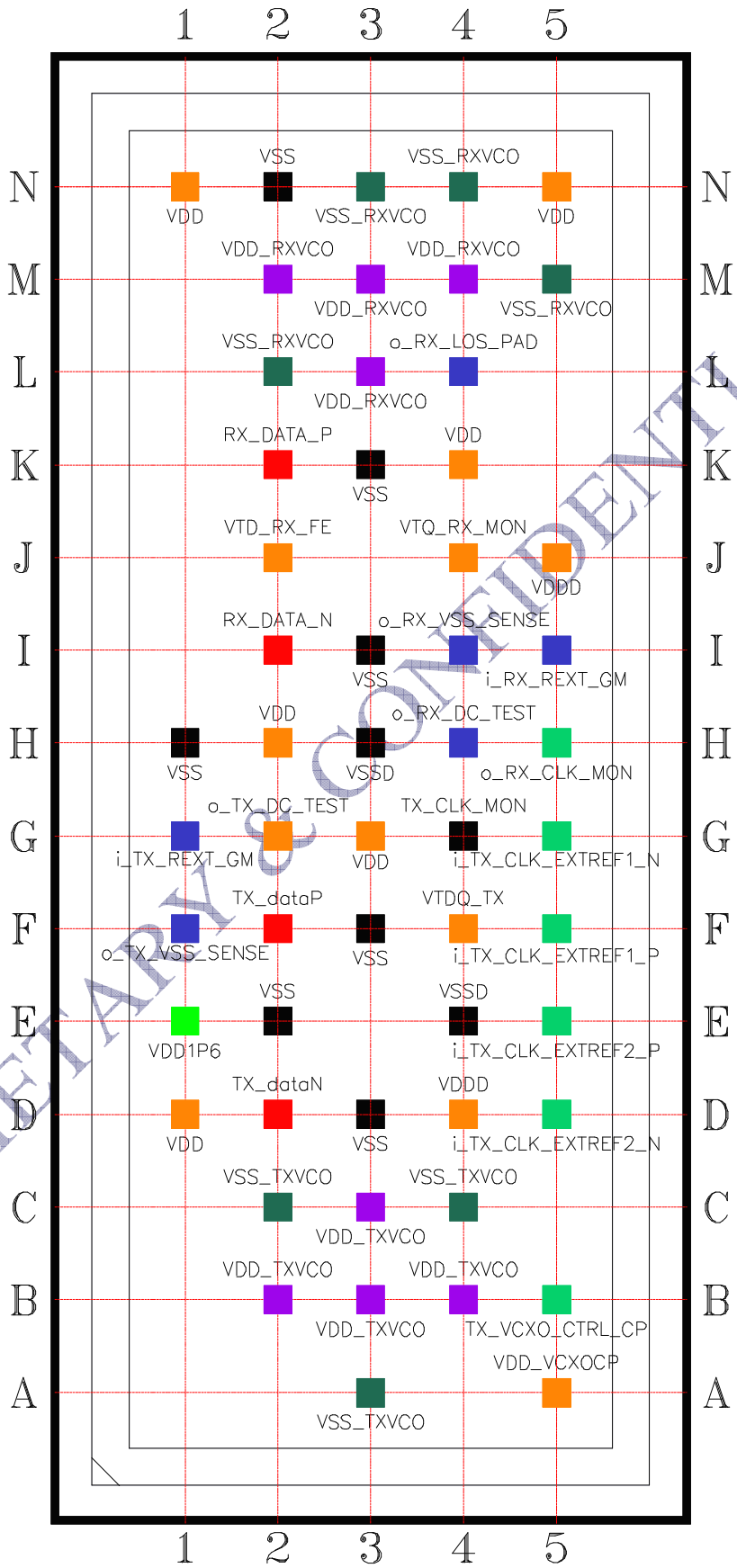

Figure 3. Bump-out diagram

Table 2. Electrical absolute maximum ratings

Description	Min	Max	Units
Power supply VDD	-0.5	1.5	V
Power supply VDDD	-0.5	1.5	V
Power supply VDD_VCO	-0.5	1.5	V
Power supply VDD_VCXOCP	-0.5	1.5	V
Power supply VDD_1P6	-0.5	2.0	V
CMOS 1.8V Control input voltage	-0.5	2	V
CMOS 3.3V Control input voltage (optional)	-0.5	4	V
Junction temperature	-55	125	ºC
End Of Life (EOL)	10		years

DC Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes
Power Supply					
Power Supply (VDD)	1.14	1.20	1.26	V	
Power Supply (VDDD)	1.08	1.20	1.32	V	
Power Supply (VDD_VCO)	1.14	1.20	1.26	V	
Power Supply (VDD_VCXOCP)	1.14	1.20	1.26	V	
Power Supply (VDD_1P6)	1.52	1.60	1.80	V	
Power Supply Current		150*		mA	
Termination Resistance at the Input (SE)	43	50	59	Ω	Limited by process variation over $\pm 3\sigma$
Termination Resistance at the Output (SE)	43	50	59	Ω	Limited by process variation over $\pm 3\sigma$
Analog core Logic I/O					
Digital input voltage high	0.9	1.2	1.32	V	
Digital input voltage low		0.0	0.32	V	
Digital output voltage high	0.9	1.2	1.32	V	
Digital output voltage low		0.0	0.32	V	
Clock monitors output					
Output swing (single-ended)		400		mVpp	Outputs terminated to 50Ω
Output common mode		1125		mV	

NOTE: Main operation mode.

Table 4. AC Electrical Specifications

I/O Port	Parameter	Symbol	Min.	Typ.	Max.	Units
Deserializer						
Data inputs **i_DATA_P** **i_DATA_N**	**Line rate**	f_b	8.5	10.3	11.3	Gb/s
	Impedance Terminated to VTDQ	R_{DIN}		50		Ω
	Return Loss 50MHz-10GHz	S_{11}			-10	dB
	Input swing (SE)		15		500	mV, p-p
Data outputs **o_DATA<0:31>**	**Output data rate per channel**		8.5/32	10.3/32	11.3/32	Gb/s
	Output data swing			1.2		V
Clock inputs **i_CLK_REF1_P** **i_CLK_REF1_N**	**Clock frequency**	F_{CLKI}		f_b/64		GHz
	Amplitude	I_{CLK0}		0.4		mA
	Impedance	R_{CLKI}		1.5		kΩ
Clock output **o_RckMon**	**Clock frequency**		f_b/16320		f_b/16	GHz
	Impedance Terminated to VTQ_MON			50		Ω
	Output swing			250		mV, p-p

I/O Port	Parameter	Symbol	Min.	Typ.	Max.	Units
Serializer						
Data output **o_DATA_P** **o_DATA_N**	**Data rate**	f_b	8.5	10.3	11.3	Gb/s
	Impedance	R_{DOUT}		50		Ω
	Return Loss (50 MHz-10GHz)	S_{11}			-10	dB
	Output swing (SE) (nominal)			400	500	mV, p-p
	Output swing (SE) (reduced)			250		mV, p-p
	Output common mode			1.2		V
Data input **i_DATA<1:32>**	**Input data rate**		8.5/32	10.3/32	11.3/32	Gb/s
	Input data swing			1.2		V
Clock inputs **i_CLK_EXTREF1_P** **i_CLK_EXTREF1_N** **i_CLK_EXTREF2_P** **i_CLK_EXTREF2_N**	**Clock frequency**	F_{CLKI}		f_b/64		GHz
	Amplitude	I_{CLKI}		0.4		mA
	Impedance	R_{CLKI}		1.5		kΩ
Clock output **o_CLK_MON**	**Clock frequency**		f_b /16320		f_b /16	GHz
	Impedance **Terminated to VTQ_MON**			50		Ω
	Output swing			250		mV, p-p
	Output common mode			1125		mV

Simulation schematic for the macro block is shown in Figure 4.

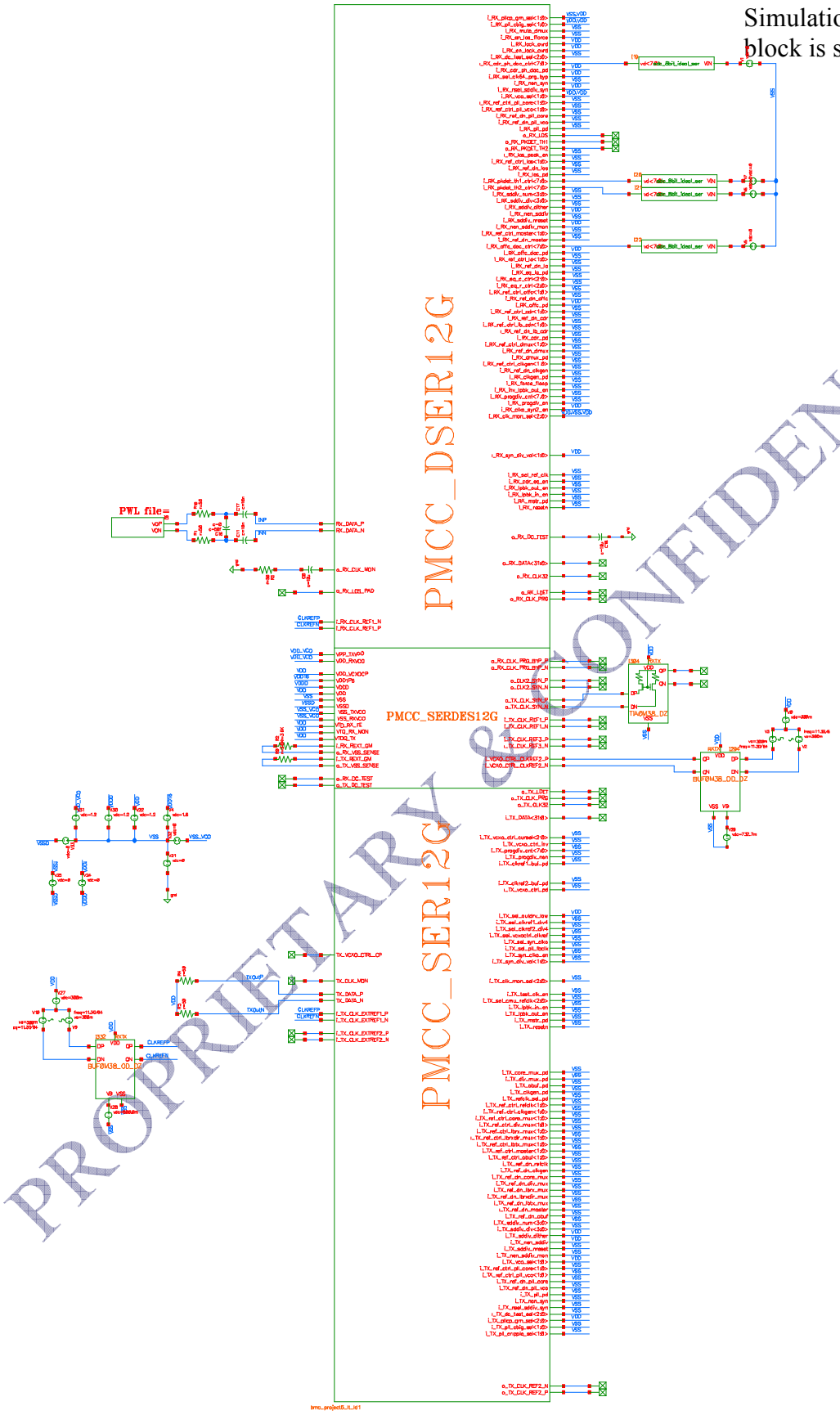

Figure 4. IP block simulation and test schematics

MACRO LAYOUT VIEW

PMCC_SERDES12G macro layout is optimally designed taking symmetry, parasitic capacitances, inductance and reliability into account. Layout design leverages all 8 metal layers available in the IBM10LPE process 5_01_00_01_LD metal stack. Compact layout ensures minimum parasitic capacitance, inductance, device mismatch and minimum die area.

Layout considerations for macro integration:

- OA is used for ground connections to minimize "ground bounce" effects.
- BA is used for VDD, VDDD, VDD_VCO connection.
- Other layout features incorporated by customer into or adjacent to macro can affect macro performance and should be carefully analyzed.
- Upon request, PMCC can provide IP for different metal stack, can change the macro block shape or migrate the macro block to different process.

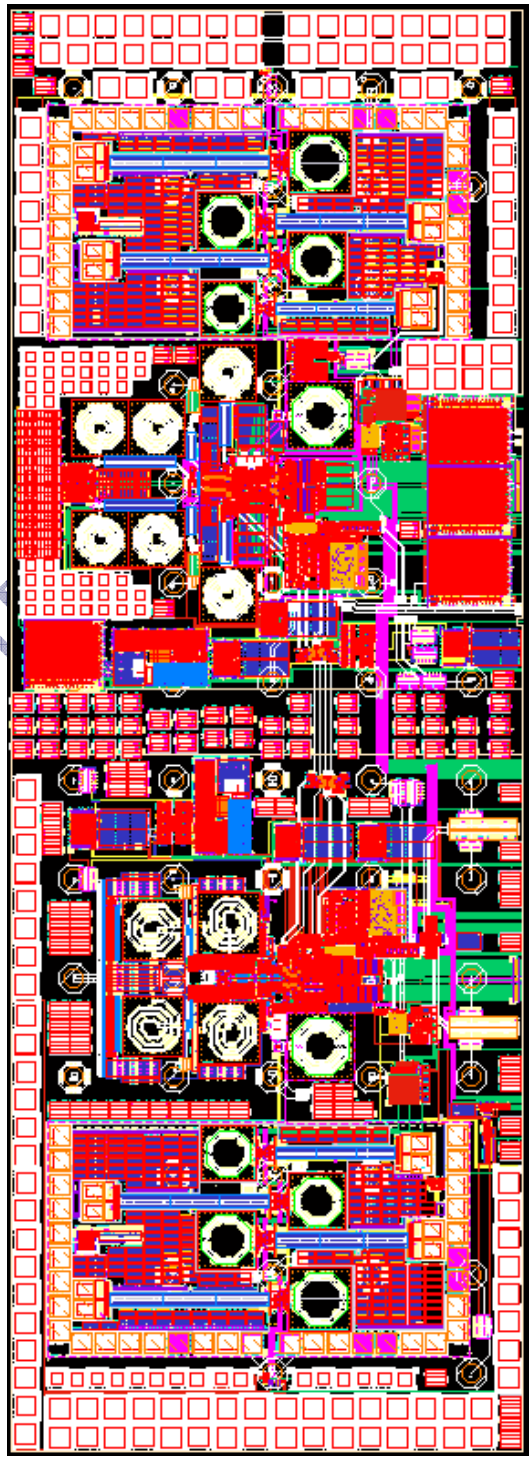

Figure 5. PMCC_SERDES12G macro core layout view. Note: some of the details and/or layers might be omitted. Layout size is 3643µm x 1289µm.

Table 5 Version Control

Revision	Date	Author	Changes
V1.0	03/26/10	PMCC	Initial version of the document
V1.1	03/30/10	PMCC	Corrected Table 4. Reviewed macro description

