Serializer 32:1 for 8.5-11.3Gb/s PMCC_SER12G

IP MACRO **Datasheet Rev 1.0**

Process: 65nm IBM CMOS10LPE

DESCRIPTION

PMCC_SER12G is a macro-block designed for robust 8.5-11.3Gb/s data 32:1 serialization independent on data coding. The serializer (except 32 bit inputs) is implemented based on differential CML logic for robust operation under strong noise coupling through power, ground and substrate. The 32 bit wide data stream (CMOS levels) coming from a FEC or another digital block is converted to differential CML levels, serialized and retimed to remove even/odd bit distortion, shape the eye and remove jitter. Serial data is shipped out through a differential 50Ω terminated (each output) data buffer. Multiple dividers (including fractional N) are implemented for support of different clocking modes: 79:85, 85:79 (FEC+G.709) 14:15, 15:14 (FEC only) 237:239, 239:237 (G.709 only) 255:239, 239:255 (add FEC to G709 frame) when macro is integrated with a complimentary deserializer. All biasing currents are programmable within +/-30% for operational margin estimation. DC test points permit to measure internal temperature, bias voltages and ground potential. Loop-back I/Os are integrated for link testing purposes. VCXO PLL is included for convenient reference clock generation by using an external high quality oscillator. Layout is designed using IBM CMOS10LPE 5_01_00_01_LD metal stack. Control functions and layout configuration can be customized upon special agreement.

APPLICATIONS

SONET/SDH OC-192 transmitter PHY
10Ge transmitter with serializer
10G back planes
XFI transmitter with serialization (both line and host side)

FEATURES

- Data-rates from 8.5Gb/s to 11.3Gb/s.
- Digital 32-bit input
- Output CML 50Ω terminated
- Output swing 400mV or 250mV p-p SE
- Output data line rate retiming
- Low power consumption (110mW)
- 1.2V and 1.8V power supplies
- Clock synthesizer (including ∑Δ)
- LOL detection
- Adjustable (+/-30%) bias currents
- DC test points.
- Integrated temperature sensor
- Stand-by mode
- Loop back signal input/output.
- Clock monitor output
- VCXO control PLL

PMCC_SER12G BLOCK DIAGRAM

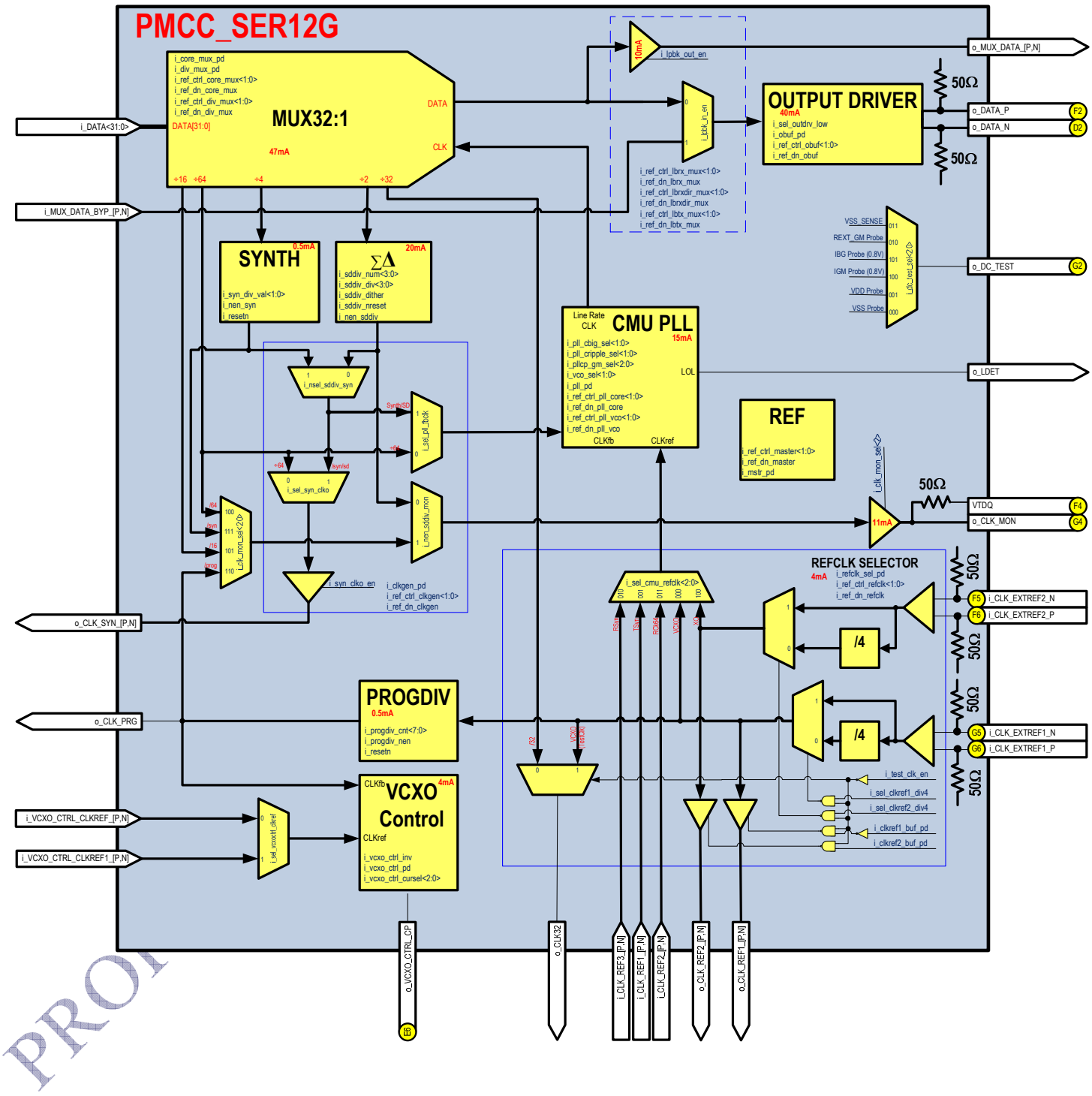

Figure 1. PMCC_SER12G block diagram

MACRO SCHEMATIC SYMBOL. PIN DESCRIPTION.

Table 1 Pin Descriptions

Name	Pin #	Description	Function
o_MUX_DATA_P		Serializer line rate data output for on-chip loopback or custom functionality enablement. Direct polarity	Analog output
o_MUX_DATA_N		Serializer line rate data output for on-chip loopback or custom functionality enablement. Inverted polarity	Analog output
i_MUX_DATA_BYP_P		Serializer output bypass input for loopback or custom functionality enablement. Direct polarity	Analog input
i_MUX_DATA_BYP_N		Serializer output bypass input for loopback or custom functionality enablement. Inverted polarity	Analog input
o_CLK_REF2_P		External reference clock #2 pass through output with optional /4. Direct output	Analog output
o_CLK_REF2_N		External reference clock #2 pass through output with optional /4. Inverted output	Analog output
o_CLK_REF1_P		External reference clock #1 pass through output with optional /4. Direct output	Analog output
o_CLK_REF1_N		External reference clock #1 pass through output with optional /4. Inverted output	Analog output
i_VCXO_CTRL_CLKREF1_P		VCXO PLL reference clock input #1. Direct polarity	Analog input
i_VCXO_CTRL_CLKREF1_N		VCXO PLL reference clock input #1. Inverted polarity	Analog input
i_CLK_REF2_P		Internal PLL reference clock #2 input. Direct polarity	Analog input
i_CLK_REF2_M		Internal PLL reference clock #2 input. Inverted polarity	Analog input
i_CLK_EXTREF2_P	F6	External PLL reference clock #2 input routed to bump. 50Ω terminated. Direct polarity	Analog output
i_CLK_EXTREF2_N	F5	External PLL reference clock #2 input routed to bump. 50Ω terminated. Inverted polarity	Analog input
i_CLK_EXTREF1_P	G6	External PLL reference clock #1 input routed to bump. 50Ω terminated. Direct polarity	Analog input
i_CLK_EXTREF2_N	G5	External PLL reference clock #1 input routed to bump. 50Ω terminated. Inverted polarity	Analog input
o_VCXO_CTRL_CP	E6	VCXO control charge pump output routed to a bump	Analog output
o_DC_TEST		DC Test Point Multiplexer to output routed to a bump	Analog output
o_CLK_MON	G4	Clock monitor signal routed to output routed to a bump	Analog output CML output
o_DATA_P	F2	line rate serial data output produced by serializer 32:1. Direct output routed to bump	High speed Analog output
o_DATA_N	D2	line rate serial data output produced by serializer 32:1. Inverted output routed to bump	High speed Analog output
i_CLK_REF1_P		Internal PLL reference clock #1 input. Direct polarity	Analog input
i_CLK_REF1_N		Internal PLL reference clock #1 input. Inverted polarity	Analog input
o_CLK_SYN_P		#1 clock synthesizer direct output	Analog Output
o_CLK_SYN_N		#1 clock synthesizer inverted output	Analog Output
i_CLK_REF3_P		Internal PLL reference clock #3 input. Direct polarity	Analog input
i_CLK_REF3_N		Internal PLL reference clock #3 input. Inverted polarity	Analog input
i_VCXO_CTRL_CLKREF2_P		VCXO PLL reference clock input #2. Direct polarity	Analog input
i_VCXO_CTRL_CLKREF2_N		VCXO PLL reference clock input #2. Inverted polarity	Analog input
i_test_clk_en		Test clock enable signal	Digital input

i_vcxo_ctrl_inv		VCXO reference tuning slope inversion signal	Digital input
i_sel_outdrv_low		High state will put CML output buffer in low-swing output mode	Digital input
i_vcxo_ctrl_pd		Reference clock controller power down	Digital input
i_sel_vcxoctrl_clkref		Programmable reference clock source selection signal	Digital input
i_sel_syn_clko		Synthesized reference clock output (0=/64, 1=/synth)	Digital input
i_sel_pll_fbck		Reference clock input selection signal (0=/64, 1=/synth)	Digital input
i_syn_clko_en		Enable the output buffer of the clock synthesizer	Digital input
i_sel_clkref2_buf_pd		XO input clock division ratio (0=/64 reference, 1=/16 reference)	Digital input
i_clkref2_buf_pd		XO input clock buffer power up	Digital input
i_sel_clkref1_div4		VCXO input clock division ratio (0=/64 reference, 1=/16 reference)	Digital input
i_clkref1_buf_pd		VCXO output buffer power down	Digital input
i_clk_mon_sel<2:0>		The receiver clock monitor selector control	Digital input
i_vcxo_ctrl_cursel<2:0>		Biasing current adjustment for VCXO	Digital input
i_progdiv_cnt<7:0>		The signal representing number by which the CLK/16 will be divided by the programmed divider	Digital input
i_progdiv_nen		Programmable Divider disable signal	Digital input
i_syn_div_val<1:0>		Clock synthesizer clock division ratio	Digital input
i_lpbk_in_en		Enable signal of loopback between CDR and CMU	Digital input
i_lpbk_out_en		Enable signal of loopback between CMU and CDR	Digital input
i_mstr_pd		Power down of all current references and the IP MACRO	Digital input
i_resetn		Input for resetting the internal IP MACRO state	Digital input
i_sel_cmu_refclk<2:0>		Reference clock selection signal	Digital input
o_LDET		CDR PLL Lock detector full swing CMOS output. "1" indicates lock	Digital output
o_CLK_PRG		Full swing CMOS programmable divider output	Digital output
o_CLK32		Full swing CMOS recovered /32 clock output	Digital output
i_core_mux_pd		Multiplexer power down	Digital input
i_div_mux_pd		Power down of clock frequency dividers for multiplexer core	Digital input
i_obuf_pd		Power-down of Output Buffer	Digital input
i_clkgen_pd		Clock generator power down	Digital input
i_refclk_sel_pd		Power down of reference clock selector	Digital input
i_ref_ctrl_refclk<1:0>		The CMU biasing current adjustment	Digital input
i_ref_ctrl_clkgen<1:0>		The Clock Synthesizer biasing current adjustment	Digital input
i_ref_ctrl_core_mux<1:0>		Multiplexer biasing current adjustment	Digital input
i_ref_ctrl_div_mux<1:0>		Biasing current adjustment for Multiplexer's dividers	Digital input
i_ref_ctrl_lbrx_mux<1:0>		Biasing current adjustment for Loopback with RX circuit	Digital input
i_ref_ctrl_lbrxdir_mux<1:0>		Biasing current adjustment for Loopback with RX circuit	Digital input
i_ref_ctrl_lbtx_mux<1:0>		Biasing current adjustment for Loopback with RX CDR circuit	Digital input
i_ref_ctrl_master<1:0>		The current reference current adjustment	Digital input
i_ref_ctrl_obuf<1:0>		Biasing current adjustment for Output Buffer	Digital input
i_ref_dn_refclk		Biasing power down for Clock Selector	Digital input
i_ref_dn_clkgen		Biasing power down for Clock Generator	Digital input
i_ref_dn_core_mux		Biasing power down for Multiplexer Core	Digital Input
i_ref_dn_div_mux		Biasing power down for Multiplexer Dividers	Digital Input
i_ref_dn_lbrx_mux		Biasing power down for Loopback	Digital Input

i_ref_dn_lbrxdir_mux		Biasing power down for Loopback	Digital Input
i_ref_dn_lbtx_mux		Biasing power down for Loopback	Digital Input
i_ref_dn_master		Biasing power down for Current References	Digital Input
i_ref_dn_obuf		Biasing power down for Output Buffer	Digital Input
i_sddiv_num<3:0>		The division ration setting inputs. Division ratio is set by num/div/32	Digital input
i_sddiv_div<3:0>			Digital input
i_sddiv_dither		Dithering control enable for Sigma-Delta Divider	Digital input
i_nen_sddiv		Sigma-Delta Divider enable	Digital input
i_sddiv_nreset		Sigma-Delta Divider reset signal	Digital input
i_nen_sddiv_mon		Sigma-Delta Divider output monitor	Digital input
i_vco_sel<1:0>		Input for selecting the VCO frequency	Digital input
i_ref_ctrl_pll_core<1:0>		Biasing current adjustment for PLL core	Digital input
i_ref_ctrl_pll_vco<1:0>		Biasing current adjustment for PLL VCO	Digital input
i_ref_dn_pll_core		Biasing current power down for PLL Core	Digital input
i_ref_dn_pll_vco		Biasing current power down for PLL VCO	Digital input
i_pll_pd		Power down for PLL	Digital input
i_nen_syn		Synthesizer disablement signal	Digital input
i_nsel_sddiv_syn		Clock synthesizer selection for clock generation	Digital input
i_dc_test_sel<2:0>		Input signal determining the DC Test point channel	Digital input
i_pllcp_gm_sel<2:0>		Gain control bus for PLL CMU	Digital input
i_pll_cbig_sel<1:0>		Integrating capacitance selection in PLL CMU	Digital input
i_pll_cripple_sel<1:0>		PLL loop filter ripple capacitor selection	Digital input
i_DATA<31:0>		Serializer 32:1 input data stream. Full swing CMOS output	Digital input
VTDQ	F4	Power for 50Ohm output termination resistors	Power input
VDD_VCXOCP	D6	1.2V analog power for VCXOCP	Power input
VDD18	E1	1.8V analog power supply for Output Driver	Power input
VDD	D1, D4, G3	1.2V analog power supply	Power input
VDDD	?	1.2V digital power supply	Power input
VDD_VCO	B2, B3, B4, C3	1.2V analog power supply for VCO	Power input
REXT_GM	G1	External resistor bump pad connection	Analog input
VSS_SENSE	F1	Common node sensing bump pad	Analog input
VSS	D3, E4, F3	Common node for analog units	Ground input
VSSD		Common node for digital units	Ground input
VSS_VCO	A3, C2, C4	Common node for VCO	Ground input

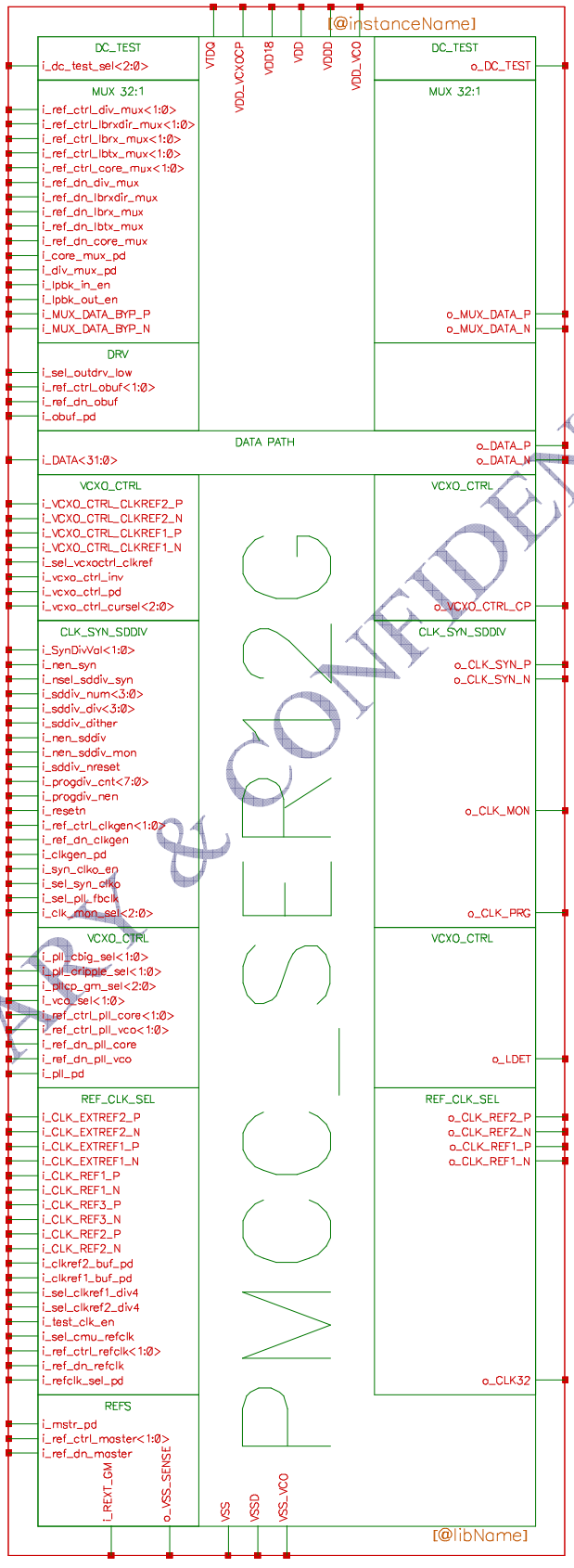

Figure 2 Macro schematic symbol

BUMP-OUT_DIAGRAM

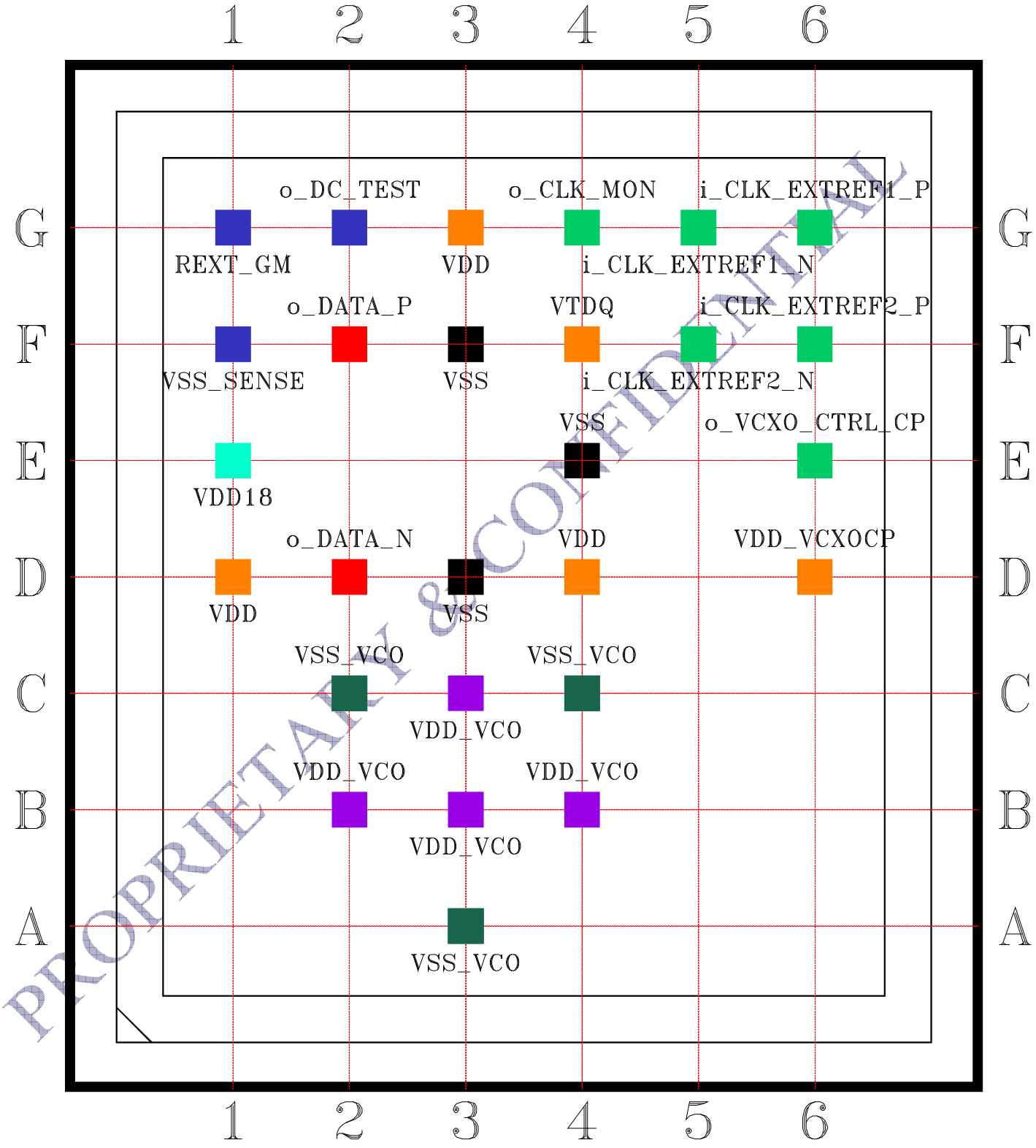

Figure 3. Bump-out diagram

Table 2. Electrical absolute maximum ratings

Description	Min	Max	Units
Power supply VDD	-0.5	1.5	V
Power supply VDDD	-0.5	1.5	V
Power supply VDD_1P8	-0.5	2	V
Power supply VDD_VCO	-0.5	1.5	V
Power supply VDD_VCXOCP	-0.5	1.5	V
CMOS 1.8V VCXO control input voltage	-0.5	2	V
CMOS 1.8 to 3.3V control input voltage	-0.5	4	
Junction temperature	-55	125	ºC
End Of Life (EOL)	10		years

DC Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes
Power Supply					
1.2V analog supply voltage (VDD)	1.14	1.2	1.26	V	
1.2V digital supply voltage (VDDD)	1.14	1.2	1.26	V	
1.8V analog supply voltage (VDD_1P8)	1.71	1.8	1.89	V	
1.2V voltage for VCO (VDD_VCO)	1.14	1.2	1.26	V	
1.8V-3.3V voltage for VCXO_CTRL (VDD_VCXOCP)	1.7	1.8	3.5	V	
1.2V Power Supply Current		64*		mA	
1.8V Power Supply Current		20*		mA	
Total Power Consumption		113*		mW	
Termination Resistance at the Data Output (SE)	43	50	59	Ω	Limited by process variation over $\pm 3\sigma$
Analog core Logic I/O					
Digital input voltage high	0.9	1.2	1.32	V	
Digital input voltage low	-0.3	0.0	0.32	V	
Digital output voltage high	0.9	1.2	1.32	V	
Digital output voltage low		0.0	0.32	V	

*** Main operation mode.**

Table 4 AC Electrical Specifications

I/O Port	Parameter	Symbol	Min.	Typ.	Max.	Units
Data output **o_DATA_P** **o_DATA_N**	**Data rate**	f_b	8.5	10.3	11.3	Gb/s
	Impedance	R_{DOUT}		50		Ω
	Return Loss (50 MHz-10GHz)	S_{11}			-10	dB
	Output swing (SE) (nominal)			400	500	mV, p-p
	Output swing (SE) (reduced)			250		mV, p-p
	Output common mode			1.2		V
Data input **i_DATA<1:32>**	**Input data rate**		8.5/32	10.3/32	11.3/32	Gb/s
	Input data swing			1.2		V
Clock inputs **i_CLK_EXTREF1_P** **i_CLK_EXTREF1_N** **i_CLK_EXTREF2_P** **i_CLK_EXTREF2_N**	**Clock frequency**	F_{CLKI}		f_b/64		GHz
	Amplitude	I_{CLKI}		0.4		mA
	Impedance	R_{CLKI}		1.5		kΩ
Clock output **o_CLK_MON**	**Clock frequency**		f_b /16320		f_b /16	GHz
	Impedance **Terminated to VTQ_MON**			50		Ω
	Output swing			250		mV, p-p
	Output common mode			1125		mV

IP BLOCK TEST STRUCTURE

Simulation schematic for the test structure is shown on Figure 4. Test IC layout presented on Figure 5.

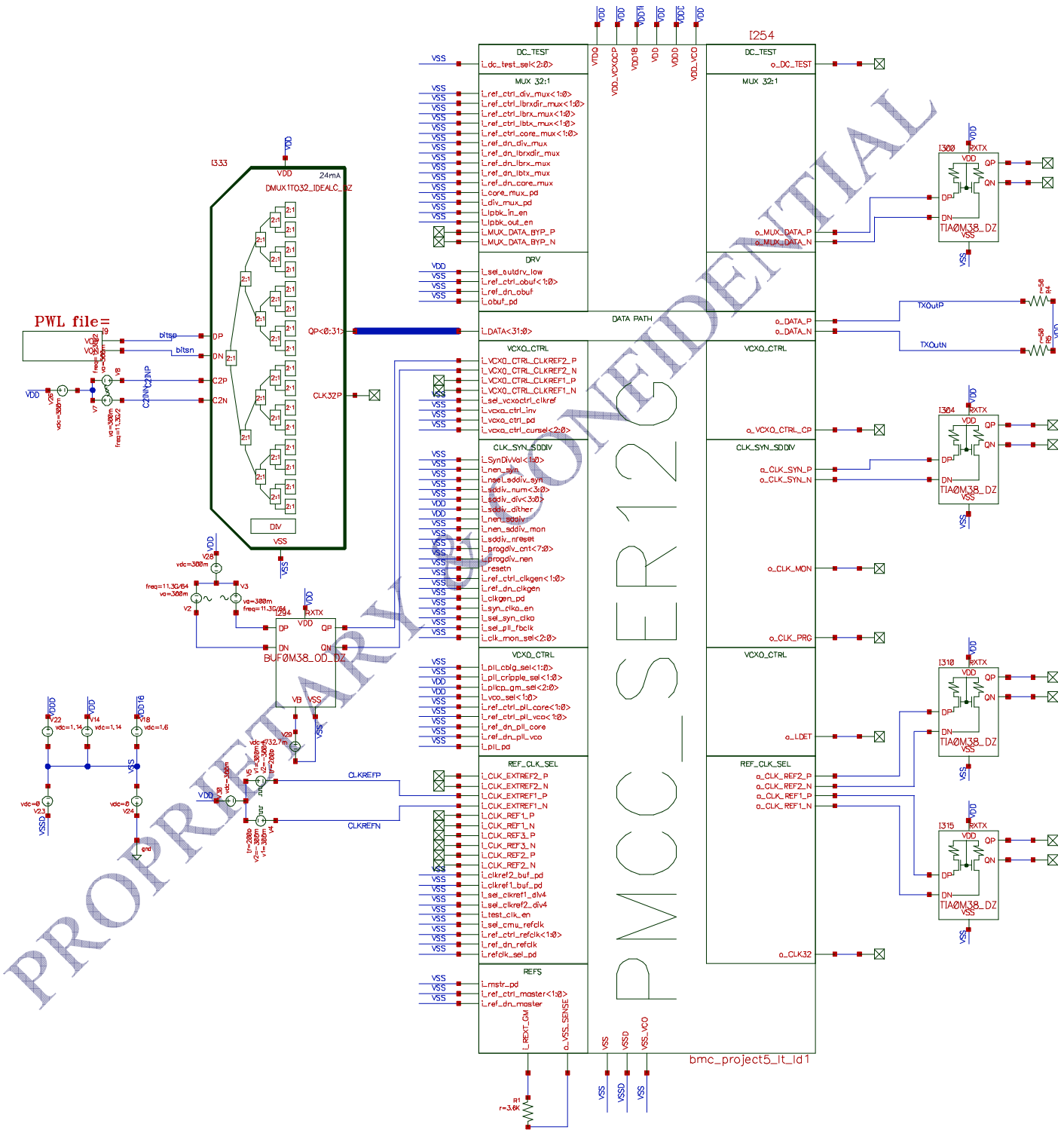

Figure 4. IP block simulation schematic

MACRO LAYOUT VIEW

PMCC_SER12G macro layout is optimally designed taking symmetry, parasitic capacitance, resistance, inductance and reliability into account. Compact layout ensures minimum power consumption by minimizing the parasitics and reduces device mismatch and layout area of the block. Layout design leverages all 8 metal layers available in the IBM 10LPE process 5_01_00_01_LD metal stack.

Layout considerations for macro integration:

- OA is used for ground connections to minimize "ground bounce" effects.
- BA is used for VDD, VDDD, VDD_VCO connection
- Other layout features incorporated by customer into or adjacent to macro can affect macro performance and should be carefully analyzed.
- Upon request, PMCC can provide IP for different metal stack, can change the macro block shape or migrate the macro block to different process.

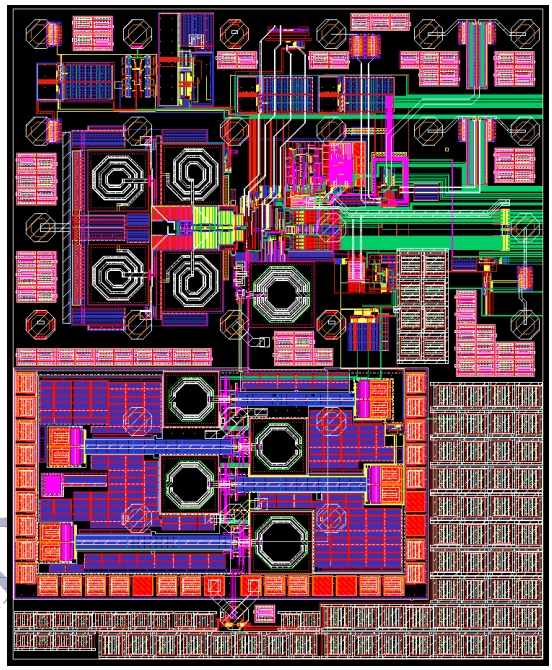

Figure 5. PMCC_SER12G macro core layout view. Note: some of the details and/or layers might be omitted. Layout size is 1360µm x 1680µm.

Table 5 Version Control

Revision	Date	Author	Changes
V1.0	03/05/10	PMCC	Initial version