Deserializer 1:32 for 8.5-11.3Gb/s PMCC_DSER12G

IP MACRO **Datasheet Rev 1.1**

Process: 65nm CMOS

DESCRIPTION

PMCC_DSER12G is a macro-block designed for robust data/clock recovery and demultiplexing 1:32. The serializer (except 32 bit outputs) is implemented based on differential CML logic for robust operation under strong noise coupling through power, ground and substrate. The data signal is applied to a 50Ω terminated data input is equalized to restore the data eye by the bandwidth limited media such as transmission lines on FR-4 PCBs or coaxial cable. The selectable equalizer can be tuned for the best performance with particular media. An automatic offset control with overriding option (manual or FEC directed) is built in for correcting of duty cycle distorted data such as in fiber optic receivers. The limiting amplifier following the equalizer is conditioning the data eye for robust CDR operation. CDR phase as well as its dynamics can be adjusted to meet specific jitter tolerance and jitter transfer specifications. Line rate data (8.5-11.3Gb/s) is deserialized to 32-bit parallel data stream and converted to CMOS format for feeding into a FEC or other digital processing block or for feeding out (LVDS output buffers are necessary). Multiple dividers (including fractional N) are implemented for support of different clocking modes: 79:85, 85:79 (FEC+G.709) 14:15, 15:14 (FEC only) 237:239, 239:237 (G.709 only) 255:239, 239:255 (add FEC to G709 frame) when macro is integrated with a complimentary serializer. All biasing currents are programmable within +/-30% for operational margin estimation in production. LOL and LOS with programmable thresholds are built in for loss of lock and loss of signal indication. DC test points are integrated for measurement of internal temperature, bias voltages and ground potential. I/Os are integrated for loop back to serializer macro for link testing purposes. Layout is designed using IBM CMOS10LPE 5_01_00_01_LD metal stack. Control functions and layout configuration can be customized upon special agreement.

FEATURES

- Data-rates from 8.5Gb/s to 11.3Gb/s.
- High sensitivity input (15mV SE p-p)
- Adjustable input signal equalizer
- Clock and Data Recovery
- Low power consumption (90mW)
- Single 1.2V Power Supply
- LOS and LOL detection
- Clock synthesizer (including ∑Δ)
- Input 50Ω termination
- Adjustable (+/-30%) reference current
- DC test points.
- Integrated temperature sensor
- Manual and automatic offset control
- Stand-by mode
- CDR bandwidth & phase adjustment.
- Loop back signal input/output.
- Clock monitor output

APPLICATIONS

SONET/SDH OC-192 receiver/CDR PHY
10Ge receiver with deserializer
10G back planes
XFI receiver with deserialization

PMCC_DSER12G BLOCK DIAGRAM

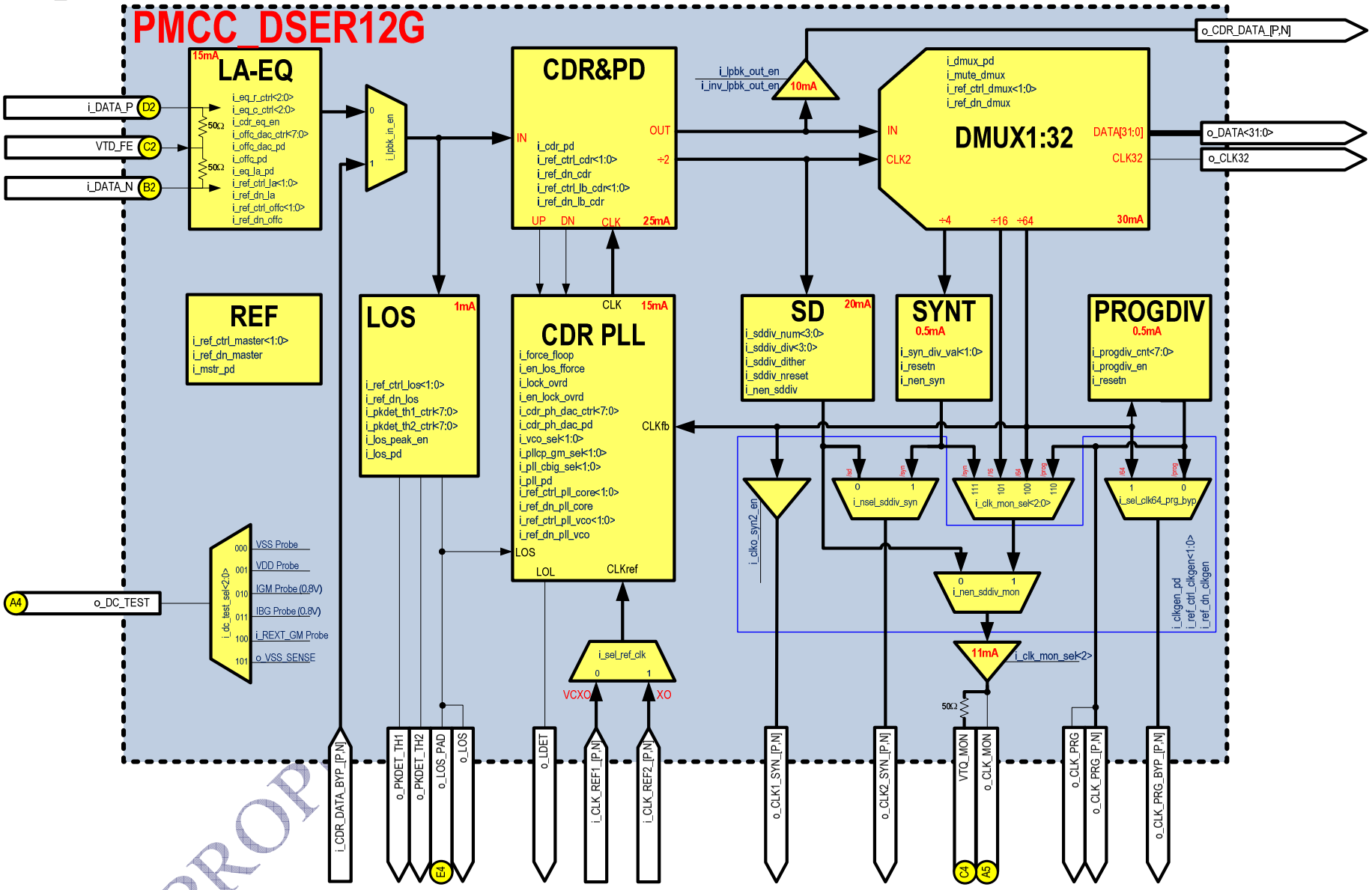

Figure 1. PMCC_DSER12G Deserializer with CDR Block Diagram

MACRO SCHEMATIC SYMBOL. PIN DESCRIPTION.

Table 1 Pin Descriptions

Name	Pin #	Description	Function
i_CDR_DATA_BYP_N		CDR detector data path bypass input for loopback or custom functionality enablement. Inverted polarity	Analog input
i_CDR_DATA_BYP_P		CDR detector data path bypass input for loopback or custom functionality enablement. Direct polarity	Analog input
i_cdr_eq_en		Signal spectrum equalization function enable	Digital input
i_cdr_pd		The Clock Data Recovery power-down	Digital input
i_cdr_ph_dac_ctrl<7:0>		CPCDR integrator current setting DAC input	Digital input
i_cdr_ph_dac_pd		CPCDR integrator current setting DAC power down	Digital input
i_clk_mon_sel<2:0>		The receiver clock monitor selector control	Digital input
i_CLK_REF1_N		CDR PLL reference clock #2 inverted input	Analog Input
i_CLK_REF1_P		CDR PLL reference clock #2 direct input	Analog Input
i_CLK_REF2_N		CDR PLL reference clock #1 inverted input	Analog Input
i_CLK_REF2_P		CDR PLL reference clock #1 direct input	Analog Input
i_clkgen_pd		The Clock Generator power-down	Digital input
i_clko_syn2_en		High state will enable the direct transfer of the recovered clock to serializer for line timing	Digital input
i_DATA_N	B2	RX frontend inverted line rate data input	Analog Input
i_DATA_P	D2	RX frontend direct line rate data input	Analog Input
i_dc_test_sel<2:0>		Signal for selection of DC Test Point channel	Digital input
i_dmux_pd		Demultiplexer power-down	Digital input
i_en_lock_ovrd		Frequency locking override signal enable signal	Digital input
i_en_los_fforce		Enables the LOS signal to be used in PLL frequency locking loop	Digital input
i_eq_c_ctrl<2:0>		The Equalizer AC response peak frequency selection	Digital input
i_eq_la_pd		The Equalizer and Limiting Amplifier power-down signal	Digital input
i_eq_r_ctrl<2:0>		The Equalizer AC response compensation	Digital input
i_force_floop		High state will force PLL's loss of lock and assert centering PLL. The lock detector is forced low	Digital input
i_inv_lpbk_out_en		High state will enable the inversion of the signal in the serial loopback	Digital input
i_lock_ovrd		Frequency locking override signal	Digital input
i_los_pd		LOS Detector power-down	Digital input
i_los_peak_en		Peak detection enable in LOS Detector	Digital input
i_lpbk_in_en		High state will enable the serial loopback circuitry	Digital input
i_lpbk_out_en		High state will enable the serial loopback circuitry	Digital input
i_mstr_pd		The power-down signal for internal reference current sources, CDR and DMUX	Digital input
i_mute_dmux		Demultiplexer data output to processing core suspend signal	Digital input
i_nen_sddiv		Sigma-Delta Divider enable	Digital input
i_nen_sddiv_mon		Sigma-Delta Divider output monitor	Digital input

i_nen_syn		Synthesizer disablement signal	Digital input
i_nsel_sddiv_syn		Clock synthesizer selection for clock generation	Digital input
i_offc_dac_ctrl<7:0>		The Offset Control DAC output current setting	Digital input
i_offc_dac_pd		The Offset Control DAC power-down	Digital input
i_offc_pd		The Offset Control power-down	Digital Input
i_pkdet_th1_ctrl<7:0>		The first threshold level setting for the peak detector	Digital input
i_pkdet_th2_ctrl<7:0>		The second threshold level setting for the peak detector	Digital input
i_pll_cbig_sel<1:0>		CPCDR integrating capacitance value selection signal	Digital input
i_pll_pd		PLL power-down	Digital input
i_pllcp_gm_sel<1:0>		CPCDR gain selection	Digital input
i_progdiv_cnt<7:0>		The signal representing number by which the CLK/16 will be divided by the programmed divider	Digital input
i_progdiv_en		Programmable Divider enable signal	Digital input
i_ref_ctrl_cdr<1:0>		The biasing current adjustment for Clock Data Recovery	Digital Input
i_ref_ctrl_clkgen<1:0>		The biasing current adjustment for Clock Generator	Digital input
i_ref_ctrl_dmux<1:0>		The biasing current adjustment for Demultiplexer	Digital input
i_ref_ctrl_la<1:0>		The biasing current adjustment for Limiting Amplifier	Digital input
i_ref_ctrl_lb_cdr<1:0>		The biasing current adjustment for Loopback circuits	Digital input
i_ref_ctrl_los<1:0>		Biasing current adjustment for LOS Detector	Digital input
i_ref_ctrl_master<1:0>		The current adjustment of internal reference current sources	Digital input
i_ref_ctrl_offc<1:0>		The biasing current adjustment for Offset Control	Digital input
i_ref_ctrl_pll_core<1:0>		PLL biasing current adjustment level control	Digital input
i_ref_ctrl_pll_vco<1:0>		PLL VCO biasing current adjustment level control	Digital input
i_ref_dn_cdr		The biasing circuit power-down for Clock Data Recovery	Digital Input
i_ref_dn_clkgen		The biasing circuitry power-down for Clock Generator	Digital input
i_ref_dn_dmux		The biasing circuitry power-down for Demultiplexer	Digital input
i_ref_dn_la		The biasing circuit power-down for Limiting Amplifier	Digital input
i_ref_dn_lb_cdr		The biasing circuitry power-down for Loopback	Digital input
i_ref_dn_los		LOS Detector biasing current power-down	Digital input
i_ref_dn_master		The power-down of internal reference current sources	Digital input
i_ref_dn_offc		The biasing circuit power-down for Offset Control	Digital Input
i_ref_dn_pll_core		PLL biasing power-down	Digital input
i_ref_dn_pll_vco		PLL VCO biasing power-down	Digital input
i_resetn		The master reset of RX internal state	Digital input
i_REXT_GM		GM reference external resistor. Connect 3.5K resistor to this pad	Analog Input
i_sddiv_dither		Dithering control enable for Sigma-Delta Divider	Digital input
i_sddiv_div<3:>		The division ration setting inputs. Division ratio is set by num/div/32	Digital input
i_sddiv_nreset		Sigma-Delta Divider reset signal	Digital input
i_sddiv_num<3:0>		The division ration setting inputs. Division ratio is set by num/div/32	Digital input
i_sel_clk64_prg_byp		High state will enable the clock pass-through	Digital input
i_sel_ref_clk		The reference clock (0=VCXO, 1=XO) selection signal	Digital Input

i_syn_div_val<1:0>		Clock synthesizer clock division ratio	Digital input
i_vco_sel<1:0>		VCO frequency selection signal	Digital input
o_CDR_DATA_N		CDR detector recovered data inverted polarity output for loopback or custom functionality enablement	Analog output
o_CDR_DATA_P		CDR detector recovered data direct polarity output for loopback or custom functionality enablement	Analog output
o_CLK_MON	A5	Clock monitoring routed to a bump	Analog Output
o_CLK_PRG		Full swing CMOS programmable divider output	Analog output
O_CLK_PRG_BYP_N		programmable divider inverted clock output with bypass by recovered /64 clock option	Analog Output
O_CLK_PRG_BYP_P		programmable divider direct clock output with bypass by recovered /64 clock option	Analog Output
o_CLK_PRG_N		Programmable divider inverted clock output	Analog Output
o_CLK_PRG_P		Programmable divider direct clock output	Analog Output
o_CLK1_SUN_N		#1 clock synthesizer inverted output	Analog Output
o_CLK1_SYN_N		Programmable divider inverted clock output	Analog Output
o_CLK1_SYN_P		#1 clock synthesizer direct output	Analog Output
o_CLK1_SYN_P		Programmable divider direct clock output	Analog Output
o_CLK2_SYN_N		#2 clock synthesizer inverted output	Analog Output
o_CLK2_SYN_P		#2 clock synthesizer direct output	Analog Output
o_CLK32		Full swing CMOS recovered /32 clock output	Analog output
o_DATA<31:0>		Recovered and de-serialized 1:32 data stream full swing CMOS output; retimed and matched with o_CLK32	Analog output
o_DC_TEST	A4	DC test point output routed to a bump	Analog Output
o_LDET		CDR PLL Lock detector full swing CMOS output. "1" indicates lock	Analog output
o_LOS		LOS detector full swing CMOS output. "1" indicates loss of signal	Digital output
o_LOS_PAD		buffered LOS detector full swing CMOS output routed to a bump. "1" indicates loss of signal	Digital output
o_PKDET_TH1		RX frontend LOS peak detector digital output. "1" indicates input signal above programmable threshold level 1	Analog output
o_PKDET_TH2		RX frontend LOS peak detector digital output. "1" indicates input signal above programmable threshold level 2	Analog output
o_VSS_SENSE	B4	RX ground return path for GM reference external resistor	Analog output
VDD	G1, A2, D4, G5	1.2V analog power supply	Analog Power
VDD_VCO	F2, F3, F4, E3	1.2V analog power supply for VCO	Analog power
VDDD	C5	1.2V digital power supply	Digital Power
VSS	A1, G2, B3, D3	Common node for analog units	Analog power
VSS_VCO	E2, G3, G4, F5	Common node for VCO	Analog power
VSSD	A3	Common node for digital units	Analog power
VTD_FE	C2	1.2V analog power supply for input termination resistors	Analog Power
VTQ_MON	C4	1.2 analog power supply for clock monitoring output termination resistors	Analog Power

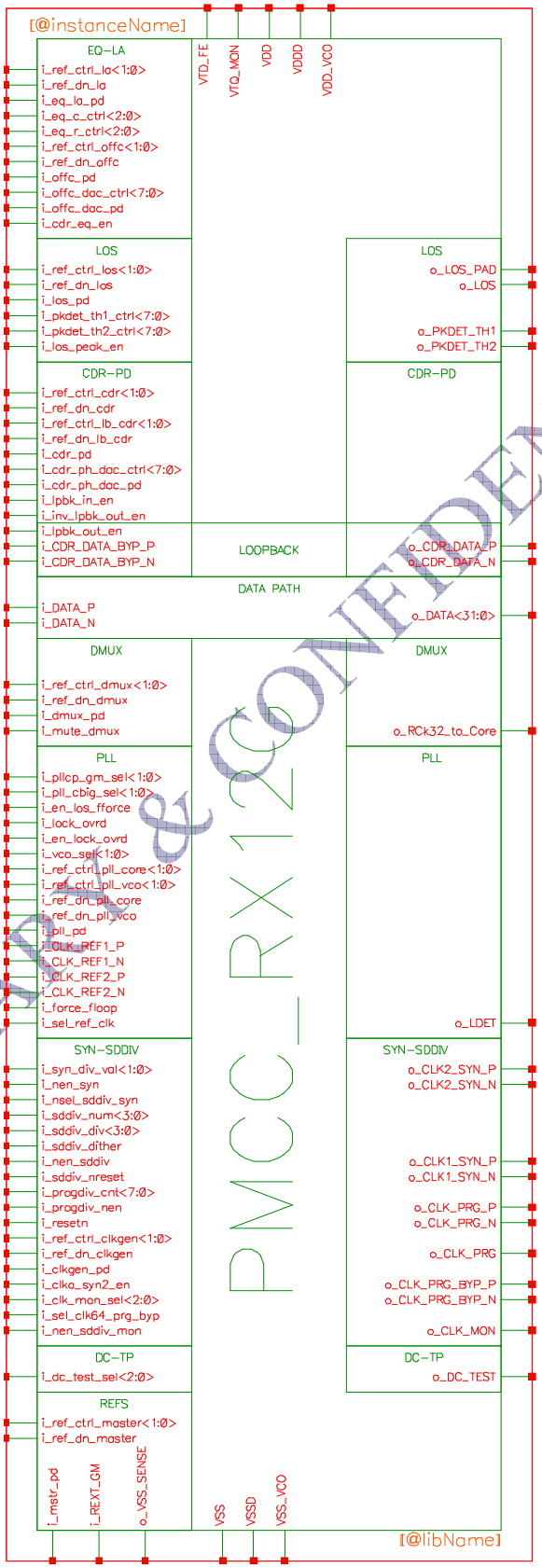

Figure 2. Macro schematic symbol

BUMP-OUT DIAGRAM

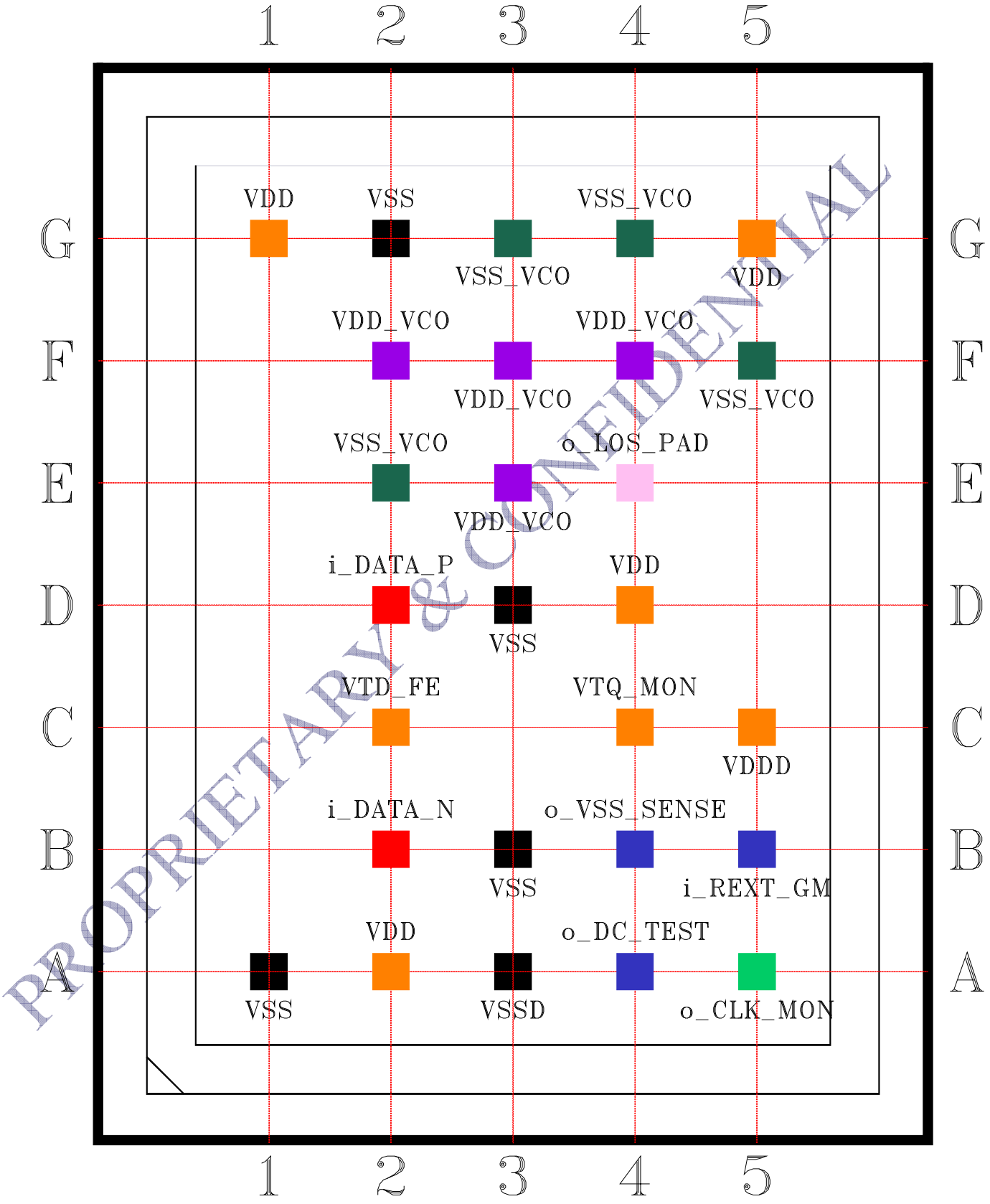

Figure 4. Bump-out diagram

Table 2. Electrical absolute maximum ratings

Description	Min	Max	Units
Power supply VDD	-0.5	1.5	V
Power supply VDDD	-0.5	1.5	V
Power supply VDD_VCO	-0.5	1.5	V
Control input voltage	-0.5	1.5	V
Junction temperature	-55	125	ºC
End Of Life (EOL)	10		years

DC Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes
Power Supply					
Power Supply (VDD)	1.14	1.20	1.26	V	
Power Supply (VDDD)	1.08	1.20	1.32	V	
Power Supply (VDD_VCO)	1.14	1.20	1.26	V	
Power Supply Current		75*		mA	
Termination Resistance at the Input (SE)	43	50	59	Ω	Limited by process variation over $\pm 3\sigma$
Analog core Logic I/O					
Digital input voltage high	0.9	1.2	1.32	V	
Digital input voltage low	-0.3	0.0	0.32	V	
Digital output voltage high	0.9	1.2	1.32	V	
Digital output voltage low		0.0	0.32	V	
Clock monitors output					
Output swing (single-ended)		400		mVpp	Outputs terminated to 50Ω
Output common mode		1125		mV	

*** Main operation mode.**

Table 4 AC Electrical Specifications

I/O Port	Parameter	Symbol	Min.	Typ.	Max.	Units
Data inputs	**Line rate**	f_b	8.5	10.3	11.3	Gb/s
i_DATA_P **i_DATA_N**	**Impedance** Terminated to VTDQ	R_{DIN}		50		Ω
	Return Loss 50MHz-10GHz	S_{11}			-10	dB
	Input swing (SE)		15		500	mV, p-p
Data outputs **o_DATA<0:31>**	**Output data rate per channel**		8.5/32	10.3/32	11.3/32	Gb/s
	Output data swing			1.2		V
Clock inputs	**Clock frequency**	F_{CLKI}		$f_b/64$		GHz
	Amplitude	I_{CLK0}		0.4		mA
i_CLK_REF1_P **i_CLK_REF1_N**	**Impedance**	R_{CLKI}		1.5		kΩ
Clock output	**Clock frequency**		$f_b/16320$		$f_b/16$	GHz
o_RckMon	**Impedance** Terminated to VTQ_MON			50		Ω
	Output swing			250		mV, p-p

IP BLOCK SIMULATION/TEST SCHEMATICS

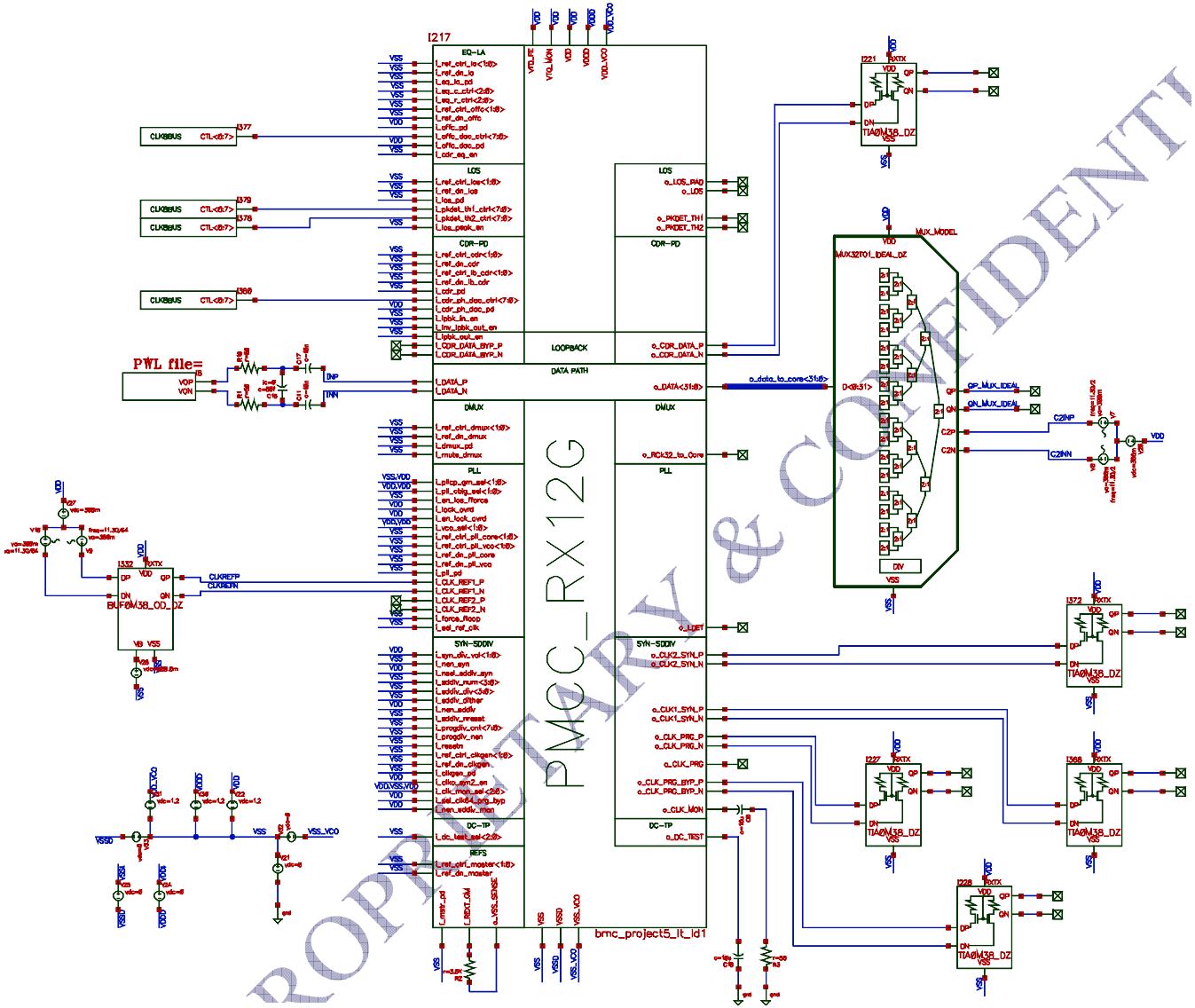

Figure 5. IP block simulation schematic

Simulation schematic for the macro block is shown in Figure 5. Macro block layout is presented in Figure 6.

MACRO LAYOUT VIEW

PMCC_DSER12G macro layout is optimally designed taking symmetry, parasitic capacitances, inductance and reliability into account. Layout design leverages all 8 metal layers available in the IBM10LPE process 5_01_00_01_LD metal stack. Compact layout ensures minimum parasitic capacitance, inductance, device mismatch and minimum die area.

Layout considerations for macro integration:

- OA is used for ground connections to minimize "ground bounce" effects.
- BA is used for VDD, VDDD, VDD_VCO connection
- Other layout features incorporated by customer into or adjacent to macro can affect macro performance and should be carefully analyzed.
- Upon request, PMCC can provide IP for different metal stack, can change the macro block shape or migrate the macro block to different process.

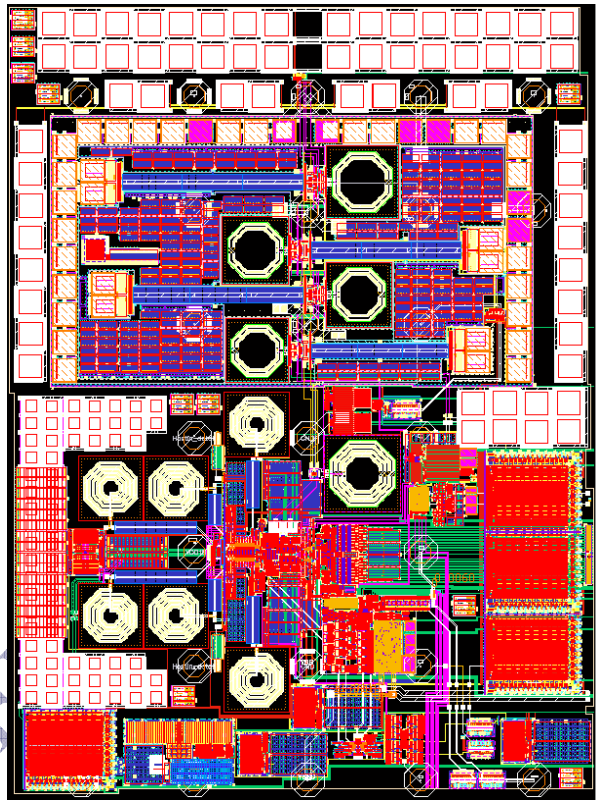

Figure 6. PMCC_DSER12G macro core layout view. Note: some of the details and/or layers might be omitted. Layout size is 1750µm x 1400µm.

Table 5 Version Control

Revision	Date	Author	Changes
V1.0	03/01/10	PMCC	Initial version of the document
V1.1	03/04/10	PMCC	Corrected IP description, data in Table 1, Table 3, Table 4.
V1.2	03/26/10	PMCC	Corrected pin description