50GHz Programmable Prescaler - Divider by 1/2/4/8/16

PMCC_DIV50G1_16

IP MACRO **Datasheet Rev 2.4**

Process: Jazz Semiconductor SBC18HX

DESCRIPTION

The PMCC_DIV50G1_16 is a high speed (up to 50GHz) fully differential programmable divider IP block, designed using Jazz SiGe120 (SBC18HX) technology. Divider selectable coefficients are /1 (bypass), /2, /4, /8 and /16. Differential architecture ensures substrate and power supply noise immunity. Macro features optional 50 Ohm terminated input and output (except bypass mode) buffer. Built-in power-down mode enables power saving in case when block is not operated. Operation frequencies, I/O signal levels, control functions and features can be customized upon special agreement.

Applications:

- Phase–locked loop (PLL) applications from DC to 50 GHz
- Point-to-point and point-to-multipoint radios
- Broadband test and measurement equipment
- Radar, electronic warfare, avionics, and space

FEATURES

- Maximum input frequency: 50GHz
- Supply voltage: 3.3V ±5%
- Power consumption:
  - / 1 : 24mW
  - / 2 : 45mW
  - / 4 : 68mW
  - / 8 : 80mW
  - /16: 94mW
- Fully differential architecture
- Layout area: 200 x 100 um

FUNCTIONAL DESCRIPTION

Differential IN_P/IN_N input signal is fed into the chain of dividers by 2. Dividers outputs are combined in the selector controlled by logic block. Division coefficient is chosen depending on B0, B1 and B2 control input state. Dividers, which are not participating in division, are powered down through PD inputs.

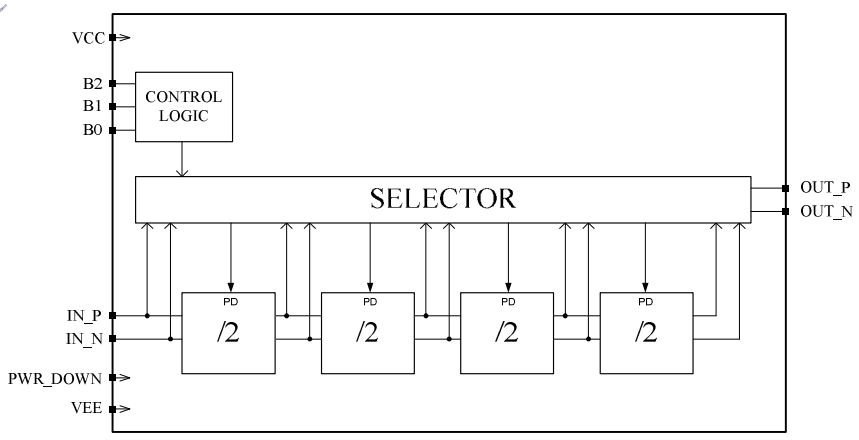

Figure 1. Programmable divider macro block diagram

MACRO SCHEMATIC SYMBOL. PIN DESCRIPTION

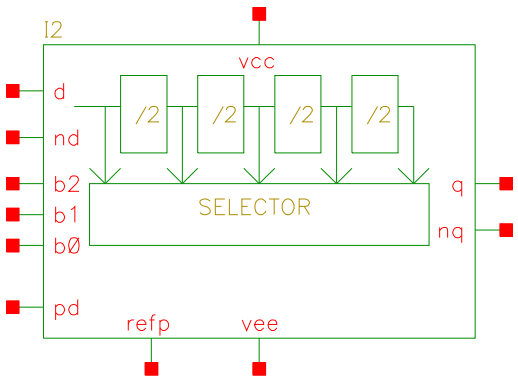

Figure 2. Macro schematic symbol

Pin Name	Description	Type
d	Direct CML input	I
nd	Inverted CML input	I
q	Direct CML output	O
nq	Inverted CML output	O
b2	Division coefficient select bit 2	CMOS
b1	Division coefficient select bit 1	CMOS
b0	Division coefficient select bit 0	CMOS
vcc	Positive power supply	PWR
vee	Ground	GND
refp	Reference voltage input	I
pd	Power down input	CMOS

AC/DC ELECTRICAL SPECIFICATIONS

Table 1. Absolute maximum ratings

Description	Min	Max	Units
Input clock voltage (pins: d,nd)	-0.5	+3.5	V
Power supply (pin vcc)	-0.5	+3.5	V
CMOS control input voltage (pins: b2, b1, b0, pd)	-0.5	+3.5	V
Reference voltage input (pin refp)	-0.5	+3.5	V
Junction temperature	-25	125	ºC
End Of Life (EOL)	10		years

DC Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. DC Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Positive power supply Vcc		3.1	3.3	3.5	V
Supply current @ Tj=125ºC	/1 (bypass)		7.2		mA
	/2		13.6		mA
	/4		20.6		mA
	/8		24.2		mA
	/16		28.5		mA
Supply current in power down state				0.1	mA
Input differential swing V_{IN_DIFF}	F_{IN}=50GHz	0.6		1.0	V
Input common mode V_{cm}		Vcc-V_{diff}/2			
Power down, b2, b1, b0 input high (Vhi)		1.7		3.5	V
Power down, b2, b1, b0 input low (Vlo)				0.5	V

Table 3. AC Characteristics

Parameter	Min	Typ	Max	Units
Input frequency*			50	GHz

* Block is subject for optimization for optimum performance at the customer selected frequency within the range as in the table.

Table 4. Division coefficient selection

Bit "b2"	Bit "b1"	Bit "b0"	Division
X	X	0	Bypass. $f_{out}=f_{in}$
0	0	1	Divide by 2
0	1	1	Divide by 4
1	0	1	Divide by 8
1	1	1	Divide by 16

MACRO LAYOUT VIEW

Divider macro layout is optimally designed taking symmetry, parasitic capacitances, inductance and reliability into account. Layout utilizes all 6 metal layers available in the SBC18HXL process. Compact layout ensures minimum parasitic capacitance, inductance and device mismatch.

Layout considerations for macro integration:

- METAL6 is used for ground connections to minimize "ground bounce" effects.
- METAL5 is used for VCC connection
- Transmission line structures should be considered for long interconnections in case of macro direct connection to IC pads (through optional 50 Ohm terminated input buffers)
- Other layout features incorporated by customer into or adjacent to macro can affect macro performance and should be carefully analyzed.

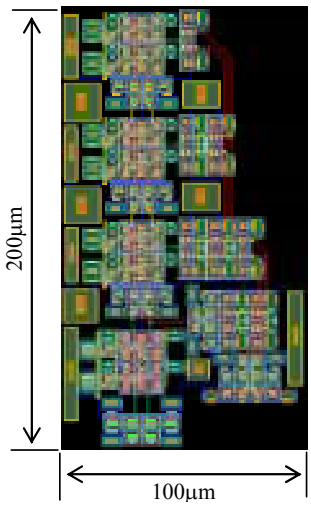

Figure 3. Macro core layout view. Note: some of the details and/or layers might be omitted.

IP BLOCK TEST STRUCTURE

Test structure consisting of divider macro, 50 Ohm terminated I/Os and reference voltage generators is shown on Figure 4. Programmable divider test IC is shown on Figure .

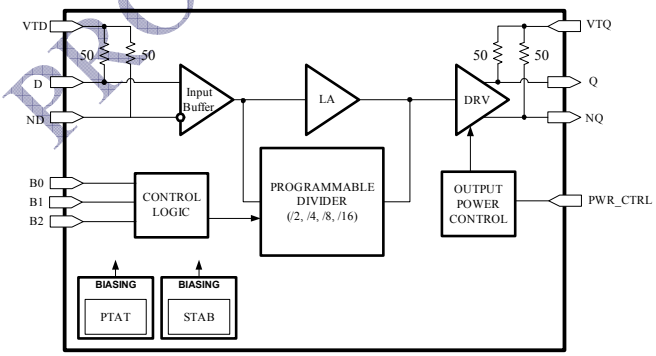

Figure 4. Macro test structure block diagram

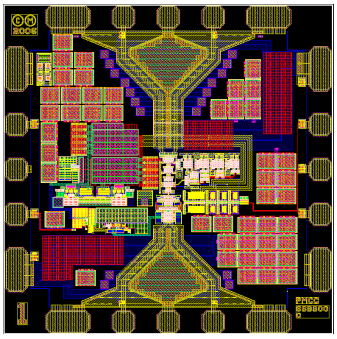

Figure 5. IP block test IC